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PROCEEDINGS OF THE NATIONAL ELECTRONICS CONFERENCE, vol. 34, 1980, pages 71-73, OAK BROOK, US; R. DANCE: "Telenet processor (TP) hardware architecture"

(73) Proprietor: **NORTHERN TELECOM LIMITED**
1600 Dorchester Boulevard West
Montreal Quebec H3H 1R1(CA)

(72) Inventor: **Jain, Prem Chand**
3552 Lancelot Court
Fremont California 94535(US)
Inventor: **Enns, Frederick**
545 Hobart Avenue
Menlo Park California 94025(US)

(74) Representative: **Crawford, Andrew Birkby et al**
A.A. THORNTON & CO. Northumberland House 303-306 High Holborn
London WC1V 7LE(GB)

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Description

The invention is in the field of switching networks for telecommunications systems, and more particularly relates to a switching network wherein digital call control signals and digital communications signals share a network bus common to both, and which accommodates communication of digital signals of asychronous and synchronous natures respectively.

The technology of telephone communications has evolved over a period of time during which telephony voice communication has been of primary concern. Telephony voice communication has been traditionally provided via circuit switched telephone facilities. Circuit switched facilities are characterized in that a circuit or a communication path is separately dedicated to each active telephone conversation throughout the entire duration of the telephone conversation. More recently communication paths have been more economically provided by respectively assigned channels in a time division multiplex (TDM) telephone exchange.

It is only in the last twenty years or so that consideration and requirements for communication systems capable of carrying a rapidly growing volume of data communication has had any significant impact on the production of communications systems in general. In contrast to the circuit switched design philosophy of telephone voice communications systems, more economical data transmission systems are typically based on a packet switching design philosphy. Packet switching is characterized in that a circuit or communication path is exclusively committed to various of data transactions one after another. Each data transaction occupies the communication path for a time which is consistent with the volume of the data divided by the bandwidth of the communication path.

Synchronous communications are most efficiently handled by circuit switched facilities. Each synchronous communication occupies a communication path or channel for the full duration of the communication without regard to utilization of bandwidth. Asynchronous communications are most efficiently handled by packet switched facilities. Each asynchronous communication, sometimes referred to as a transaction, utilizes the full bandwidth of a circuit path for only as much time as data volume divided by the bandwidth requires. Asynchronous data transmitted via circuit switched facilities seldom utilize the available bandwidth. In packet switched facilities if traffic is present the full bandwidth is used. However because of the asynchronous nature of information transfer between ports in a packet switched system, attempts to use this type of system for voice i.e. synchronous information transfers, have resulted in relatively intricate and complicated solutions which typically exhibit lesser performance than is practically acceptable. An extensive summary of the capabilities and consequences of packet switching and various exemplary systems has been documented by Roy D. Rosner under the title of "Packet Switching Tomorrow's Communications Today" and published by Lifetime Learning Publications, a division of Wadsworth, Inc., in Belmont, California.

It is apparent that asynchronous data information is inefficiently communicated by circuit switched facilities. Furthermore holding times for asynchronous data transmission in a circuit switched facility can greatly exceed the typical duration of a voice telephone conversation. Thus extensive data traffic tends to seriously congest the typical circuit switched network. It is also apparent that currently available packet switching facilities are not a practical alternative to circuit switched facilities for voice-like information as receiving delays are typically too long, and even worse are inconsistent. Thus in both public and private communications systems circuit switched facilities are typically provided. Where the occasion warrants, packet switching is provided as a separate network exclusively for asynchronous data communications.

A system that can communicate both circuit and packet switched communications is described in FR-A-2 310 594 wherein the circuit switched communications are configured by the system such that they appear as packet switched data.

A system which can communicate information from both periodic and aperiodic sources is described in WO-A-83/03328, wherein information is packetized and transmitted in accordance with a prioritizing protocol whereby in an event of collision between packets bearing periodic source data and aperiodic source data, the effect of the collision upon the packetized periodic source data is mitigated.

Summary of the Invention

It is an object of the invention to provide an improved telecommunications network capable of of operating as a packet switch and as a circuit switch.

It is also an object of the invention to provide for both packet switching and circuit switching between a plurality of units by way of a bus which is connected in common to all the units.

It is a further object of the invention to provide a bus controller being connected to the units by way of address leads and control leads in the bus, for arbitrating access to data leads in the bus for transmission of asynchronous call control signals between a call controller one of the units and other ones of the units, and for transmission of commu-

nications signals between the other ones of the units.

In accordance with the invention, a telecommunications switching network comprises: a bus comprising a group of data leads for transmission of communication signals; a plurality of units connected to the bus for transmitting and receiving asynchronous communication signals; a bus controller comprising means for defining time slot intervals for transmitting and receiving between the bus and each of the units for controlling access to the bus for transmitting the asynchronous communications signals; characterized in that: said bus controller further comprising means to define contiguously occurring frame intervals of a present number n of the time slot intervals each;
said plurality of units includes a call controller unit and at least one other unit capable of transmitting synchronous communication signals, the call controller being adapted to select one of the n time slot intervals and allocate said one time slot interval to said other unit in response to an asynchronous signal from said other unit representing a call set up request and said other unit being adapted to transmit synchronous signals in said allocated time slot interval, and to receive synchronous signals in a time slot allocated by the call controller unit;
whereby packetized data signals and synchronous signals may be interleaved during transmission via the bus.

According to one aspect of the invention the bus controller comprises a poll means for polling the units for asynchronous transmission requests; grant means for granting access to the data leads for an indefinite period of time, as required for transmission of a data packet from one of the units, sometime after an occurrence of an asynchronous transmission request from said one unit; and a synchronous cycle means being responsive to an occurrence of a synchronous request signal from any of the units, for generating a synchronous signal for a predetermined time commencing at a preset time after said occurrence, for inhibiting data packet transmission and enabling a synchronous data transmission via the data leads during said predetermined period of time.

In one example of the invention, the bus controller is connected to the units via a group of address leads and a plurality of control leads. The poll means includes a counter for periodically generating a series of addresses for polling the units one after the other. The grant means includes a queue storage means being responsive to an occurrence of an asynchronous transmission request in the form of a request flag having been asserted on a request of one of the control leads by a polled unit for storing the address corresponding to the unit. An address select means is responsive to the presence of at least one address in the queue storage means for inhibiting the address counter and for causing the address to be withdrawn from the queue storage means and to be asserted on the address leads coincident with generating a grant flag on a grant one of the control leads whereby access is granted to a unit as indicated by the asserted address.

The invention also provides a method of operating a telecommunication switching network, comprising the steps of: providing an exclusive transmission privilege for a unit having a packetized message for transmission; transmitting the packetized message while retaining said exclusive transmission privilege until the whole message has been transmitted; the method being characterized by the steps of:
periodically providing a time slot for transmission from a unit with a synchronous transmission requirement; and interrupting the transmission of a packetized message during each occurrence of said time slot and resuming the transmission of the packetized message with the next occurrence of a time slot which has not been provided for a synchronous transmission requirement.

Thus the invention may be used to operate, a telecommunications switching network to provide for transmission of signals between units connected to a bus in the switching network wherein the signals include both asynchronous call control signals for transmission between a call controller one of the units and another of the units and communication signals for transmission between calling and called ones of the other units. In the preferred method of operation a bus controller arbitrates access to the bus for signal transmission from the units by polling the units for asynchronous transmission requests and by granting access to the bus for an indefinite period of time to each of the units which has responded to being polled. The bus controller also generates frame and clock signals for defining frame periods each consisting of a plurality of bus cycles. A unit, which requires access to the bus for synchronous transmission, asserts a synchronous request signal at a predetermined time preceding a bus cycle having been designated by the call controller unit and thereafter transmits a communication signal on the bus during the designated bus cycle. A unit, which has been defined by the call controller unit as a receiver during the designated bus cycle, receives the communication signal from the bus during the d signated cycle. The remaining units including any unit having been granted access for asynchronous transmission, cease transmitting and/or receiving throughout the duration of the designated bus cycle.

Brief Description of the Drawings

An example embodiment is describ d with reference to the accompanying drawings in which:

Figure 1 is a block diagram of packet and circuit switched communications networks in accordance with the invention;

Figure 2 is a block schematic diagram of a bus controller used in figure 1 for controlling the flow of communciations through one of the networks;

Figure 3 is a block schematic diagram of poll and grant logic circuitry used in the bus controller in figure 2;

Figure 4 is a block schematic diagram of a synchronous cycle counter and generator used in the bus controller in figure 2;

Figure 5 is a block schematic diagram of error checking circuitry used in the bus controller in figure 2;

Figure 6 is a block schematic diagram of one of a plurality of a repeater circuits used in the bus controller in figure 2;

Figure 7 is a block schematic diagram of one of a plurality of segment bus unit interface circuits used in the communications networks in figure 1;

Figure 8 is an illustration of an address format for communication of packetized data via the communication networks in figure 1;

Figure 9 is an example illustration of bus protocol timing for granting bus access for communication of packetized data in the communication networks in figure 1; and

Figure 10 is an example illustration of synchronous bus cycle protocol timing for granting bus access for communication of synchronous data in the communication networks of figure 1.

Description of the Example Embodiment

In the description of the example embodiment power and ground elements required for the operation of the communications networks are neither discussed nor illustrated, as these elements are well understood by persons of typical skill in the electronic arts. Also in the interest of brevity, the generation and distribution of clock signals for the operation of the telecommunication switching network is limited to that which is convenient for an understanding of the communications networks. The embodiment illustrated in the drawings is constructed from "off-the-shelf" components, primarily silicon integrated circuits being mounted on printed circuit boards, sometimes referred to as cards. The printed circuit boards are connectable to back plane panels which carry various leads for conducting signals between the various circuit boards.

In figure 1, a redundant pair of networks, A and B, are provided for reliability. A Bus Controller A and a Bus Controller B each include a Main Bus and up to six Repeaters R, each for interfacing the Main Bus with each of up to six Segment Buses A and B respectively. An A and B pair of the Segment Buses in each Segment provide for connection at up to thirty-two Unit Locations (0-31). All of the buses include multiple conductors providing data leads and address leads which are utilized to carry digital signals in a parallel signal format as well as various control leads. Only those elements being associated with an active one of the networks A or B are normally in active use at any one time. Each of the Segment Buses is terminated remote from its associated Repeater R by a Terminator T. Each of the Terminators T provide an impedance termination for each of the conductors in the associated Segment Bus and also provides return parity indications for use in the associated bus controller. At each of the Unit Locations 0 - 31 a bus/unit interface circuit is required to provide transmitting and receiving access to the Segment Buses by means of a regimented signal protocol as illustrated in figures 9 and 10 and which is described in more detail in a later portion of the disclosure. Each of the bus/unit interface circuits is identical to the other insofar as it comprises circuitry as exemplified in figure 7. Each unit is specialized to exclusively perform one of several specific tasks. Examples of some of these tasks are as follows:

line circuit interface and synchronous signals conversion for analog telephone station sets;

line circuit interface and synchronous digital signal formation for digital telephone station sets;

asynchronous digital line circuit interface for work stations or a host computer;

digital trunk circuit circuit interface for synchronous signals;

digital trunk circuit interface for asynchronous signals;

synchronous digital signal service circuits, such as tone receiver, tone generators, etc., for providing the well-known signalling and supervisory functions required in telephone networks; and

feature interface for synchronous and asynchronous value added features for example data and/or voice messaging facilities.

The above-listed tasks are merely illustrative of the various communications services which may be provided with appropriate units by way of the networks of figure 1. One task not mentioned in the list is that of call controlling. At least one of the Unit Locations of the networks A and B is occupied by a call controller Unit. The call controller Unit is similar to a central controller in any of various computer controlled switching systems, insofar as it defines communication paths between calling and called ones of the other Units. The structure and opera-

tion of an exemplary call controller Unit or of any of the other Units is neither illustrated nor described in any detail as such is not essential to an understanding of the telecommunication network of the instant invention. It is one of the telecommunications networks of figure 1 which in itself actively provides for inter and intra Unit communications of synchronous and asynchronous digital signals. The structure and operation of the network in figure 1 is described in more detail with reference to the figures 2 - 10.

The Bus Controller in figure 2 is the source of all timing, control, and address signals which are eventually communicated via ADDRESS and control leads to an associated Segment Bus. In normal operation the Units are the sources of all response signals. The Units and the Bus Controller are sources of data information signals communicated via DATA leads.

Referring to figure 2 a bidirectional microprocessor bus 201 is connected between an eight-bit microprocessor 200, a memory 202, an interface circuit 203, a bus switchover circuit 204, a poll and grant circuit 300, a synchronous cycle counter and generator 400 and an error checking circuit 500. The memory 202 provides permanently stored program instructions defining routines implemented by the microprocessor 200 for configuring operation of the Bus Controller. In this example the microprocessor is an Intel 8031. The memory 202 also provides temporary storage for use by the microprocessor 200. The interface circuit 203 provides for data communication between the microprocessor bus 201 and the Units via DATA leads 607 in one of the segment buses as illustrated in figures 6 and 7. In figure 2, the bus switchover circuit 204 includes an input connected to a control lead 219 labelled OTHER USE, and includes an output connected to a control lead 218 labelled USE. The OTHER USE lead 219 originates with a corresponding output of a bus switchover circuit in the other Bus Controller and the USE lead 218 terminates at a corresponding input of the bus switchover circuit in the other Bus Controller. The primary function of the bus switchover circuits 204 is that of ultimately controlling which of the Bus Controllers and its associated network is in an active mode of operation and which is in a standby mode of operation. The clock generator 205 in one example consists of an internal crystal oscillator and phase lock loop circuit, not shown, which generates a clock signal on a CLOCK one of the control leads 217 and a frame signal on a FRAME one of the control leads 216. The clock generator is designed such that it has three distinct modes of operation. The first mod occurs wh n th Bus Controller is in standby operation, which is indicated by th state of the OTHER USE lead 219. In the first mode the clock generator 205 provides the clock and frame signals being synchronized with corresponding signals produced by a corresponding clock generator in the other Bus Controller. Either of the second and third modes occurs while the Bus Controller is in active opeation. In the second mode, the clock and frame signals are generated in synchronism with timing signals supplied on either of leads SYNCX and SYNCY. These timing signals originate in a remote system and are communicated via one of the Units. In the third mode, generation of the clock and frame signals depends wholly upon the free running operation of the internal oscillator. The null packet generator 206 operates substantially as a default data generator such that at times when no other element in the network is actively transmitting on the DATA leads, a null data packet is applied to the buses to prevent the DATA leads from floating. Signal assertions by the null packet generator are carried by the bus 207. Signal assertions by the null packet generator 206 are prevented in the presence of a synchronous cycle flag on a SYNCHRONOUS CYCLE lead 215.

The poll and grant circuit 300 is the source of all addresses for identifying a Unit in the network and is also the source of reset unit signals and the grant flags. The addresses are provided on the ADDRESS leads 210 and are thus distributed to each of the Bus Repeaters R and to the error check circuit 500. Operational parameters such as the range of unit addresses to be polled are determined by the microprocessor 200. However the moment to moment operation of the poll and grant circuit 300 is in response to request flags and done flags generated by the Units and received via REQUEST ones of control leads 221 and DONE ones of the control leads 225.

The synchronous cycle counter and generator 400 defines from the clock and frame signals on the CLOCK and FRAME leads 217 and 216, bus cycle occurrences in frames of bus cycles. The microprocessor 200 defines a range of bus cycles in which a synchronous transmission request received from a Unit via a SYNCHRONOUS REQUEST one of the control leads 224, may be granted via the SYNCHRONOUS CYCLE lead 215.

The error check circuit 500 monitors signals generated within the Bus Controller and signals generated in the remainder of the network to detect fault occurrences. The state of the network as determined by the error check circuit 500 is available to the microprocessor 200 via the microprocessor bus 201. Th rror check circuit 500 monitors bus cycle counting performed by the sycnchronous cycle counter and generator 400 via a bus 401, addressing performed by the poll and grant circuit 300 via the ADDRESS leads 210, data in-

formation on the bus 207, synchronous cycle flags on the SYNCHRONOUS CYCLE lead 215, control parity signals on CONTROL PARITY leads 222, and return parity signals on RETURN PARITY leads 223. The control parity and return parity signals are generated by the Teminator T. The error check circuit 500 under some detected fault condition generates an abort signal on a lead 501 for controlling operation of the poll and grant circuit 300.

The poll and grant circuit 300 is illustrated in detail in figure 3. Circuitry in the upper part of figure 3 is primarily concerned with polling Units in the network for service requests being indicated by the request flag. Circuitry in the lower portion of figure 3 is primarily concerned with storing and queuing addresses of the various Units which have asserted the request flag and ultimately satisfying each service request. In the poll and grant circuit 300 addresses are applied to the ADDRESS leads 210 from any of four sources, a poll address register 310, a reset unit address register 314, null address gates 315, and a grant address register 378. The poll address register 310 asserts an address on the ADDRESS leads 210, each time it is enabled by an address select circuit 320 via a lead 317. Addresses for the poll address register 310 are generated by a poll address counter 311 which is incremented with each enable occurrence on the lead 317. The poll address counter 311 generates sequential addresses in a range which is from time to time defined by the microprocessor 200 via the bus 201. One end of the range is stored in a minimum poll address register 313 and the other end of the range is stored in a maximum poll address register and comparator circuit 312. In operation each time the address generated in the poll address counter 311 corresponds to the maximum of the range, the maximum poll address registers and comparator circuit 312 generates a load signal which causes the poll address counter 311 to start counting from the minimum address of the range as registered in the minimum poll address register 313. The null address gates 315 are controlled by the address select circuit 320 via a lead 318 to assert a predetermined null address on the ADDRESS leads 210 during a bus cycle when no other address is asserted to activate the null packet generator 206. The reset unit address register 314 provides for a Unit reset function wherein the address of the Unit is defined by the microprocessor 200 via the bus 201 and the time at which the Unit is reset is determined by the address select circuit 320 which enables assertion on the ADDRESS leads 210 coincident with generating a reset unit flag on a RESET lead 213 in response to having received a reset request on a lead 321. An address parity generator 316 responds to each address appearing on the ADDRESS leads 210 by generating parity signals on parity ones of the ADDRESS leads 210.

Th circuitry in th lower portion of figure 3 is concerned with granting bus cycles to those Units which having been polled have asserted a request flag. An address latch 350 receives addresses on the ADDRESS leads 210 and passes these addresses via a bus 352, to a first in, first out (FIFO) select circuit 360, to a gateway and disable unit address circuit 354, and to a polling wrap around memory 357. A distinction is made between those of the Units which are specialized for larger bandwidth communications as with respect to those Units which are intended for more typical bandwidth of communications. For convenience the higher speed Units are referred to as Gateway Units and the remaining Units are referred to as Card Units. Addresses of both the Gateway Units and disabled ones of the Gateway and Card Units are defined by the microprocessor 200 and are received via the bus 201. These addresses are stored in the gateway and disable unit address circuit 354. In the event that an address on the bus 352 corresponds to one of the stored addresses, the gateway and disable unit address circuit 354 asserts a control signal on one of respective leads 355 or 356. Assuming for the moment that the control signal is not asserted, the FIFO select circuit 360 passes the address to a bus 361 and asserts a card FIFO enable signal on a lead 363. This occurs two bus cycles after the address was asserted on the address bus. If the addressed Unit has responded to the polling occurrence, a request flag is received by a request latch 364 via one of the REQUEST leads 221. The request flag is received during a bus cycle following the polling incident and a corresponding request control signal is generated on a lead 365 by the request latch 364, two bus cycles following the polling incident. A card FIFO 371 responds to the signals on the leads 363 and 365 by storing the address from the FIFO select circuit 360. Hence Card Unit addresses are queued for subsequent granting. Assuming for the moment that the control signal is asserted on the lead 355, as would be the case when the polling address on the address bus was that of a Gateway Unit, the process described immediately preceding is changed only in that the FIFO select circuit 360 asserts a gate FIFO enable signal on the lead 362, thereby causing the Gateway Unit address to be queued in a gate FIFO 370 in the presence of the request control signal on the lead 365. If on the other hand the address corresponds to that of a Unit having been defined as disabled, gateway and disable unit address circuit 354 asserts a control signal on the lead 356 and neither of the FIFOs, 370 or 371, is selected by the FIFO

select circuit 360. Hence even in the event that a disabled Unit raises a request flag, its address will not be queued for a subsequent granting. The polling wrap-around memory 357 receives the addresses from the bus 352 and request flag signals on the REQUEST leads 221. In the event that a request flag signal is received, a corresponding memory location is set and is not reset until the same address is again received in the absence of the request flag signal. When the corresponding memory location is set, the polling wrap-around memory asserts a disable signal on a lead 358, which prevents the FIFO select circuit 360 from selecting either of the FIFOs 370 and 371. Hence polling wrap-around which is characterized by more than one appearance of any one address in either of the FIFOs 370 and 371 is prevented. Each of the FIFOs 370 and 371 include full and empty output ports at which corresponding signals are asserted to indicate the state of each FIFO as being one of full of queued addresses or empty. The full ports are wire ORED on a full lead 375 which is connected to an input of the address select circuit 320. The empty ports are connected via respective empty leads 372 and 373 inputs of a grant address circuit 380. The grant address circuit 380 is responsive to grant flags on the GRANT lead 214 to generate output control signals alternately on leads 381 and 382 for causing the respective FIFOs to alternately output previously queued addresses, one after the other, onto a bus 376. If one of the FIFOs is empty only the other FIFO is caused to output the queued addresses. Each address appearing on the bus 376 is applied to the ADDRESS leads 210 via a grant address register 378 in response to the grant flag. In the event that a grant flag occurs, as in each case whereby the address select circuit 320 indicates the end of a packet transmission to the Units, and at the same time both of the FIFOs 370 and 371 are empty, the grant address circuit causes a null address to be asserted on the bus 376 by a null address source 377. In the event that a full signal is received by the address select circuit 320 polling is halted until sufficient queued addresses are applied to the address bus 210 to provide at least one address space in each of the FIFOs 370 and 371.

A primary function of the synchronous cycle counter and generator 400, illustrated in figure 4, is that of limiting synchronous access to the DATA leads 207 so that there is always some failsafe time available for asynchronous communications. A Unit may assert a synchronous request signal two bus cycles prior to a bus cycle having been assigned to it by the call control Unit. Each synchronous request is received via one of the SYNCHRONOUS REQUEST leads 224 and is latched into a synchronous cycle request latch 410 under the control of the clock signals on the CLOCK lead 217. One bus cycles later, the state of the synchronous cycle request latch 410 is applied at inputs of an AND gate 411 which passes any low signal assertion to an input of an OR gate 412. An output of the OR gate 412 is the origin of the SYNCHRONOUS CYCLE lead 215. The OR gate 412 pases the low signal assertion onto the synchronous cycle lead 215 in the event that an output of a comparator 415 is also asserted low. A frame latch 413 receives the frame signal on the FRAME lead 216 under the control of the clock signal on the CLOCK lead 217 and provides the frame signal at a clear input of a bus cycle counter 414. The bus cycle counter is operated by the clock signals on the CLOCK lead 217 to count from its cleared state of zero through to a count of 639 whereupon it is cleared by the delayed frame signal. Outputs of the bus cycle counter 414 are the origin of the bus 401. In this example the bus 401 carries ten binary signal bits in parallel for use in the error check circuit 500 and provides the eight highest order binary bits at an input A of the comparator 415. Another input B of the comparator 415 is connected, via a bus 417, to an output of a maximum cycle register 416. The maximum cycle register stores a maxim cycle number, as defined by the microprocessor 200 via the microprocessor bus 201, beyond which synchronous cycle occurrences are inhibited by the comparator 415.

The error check circuit 500, illustrated in figure 5. is primarily concerned with providing information to the microprocessor 200 with respect to various error occurrences in the network. The error check circuit 500 also generates an abort control signal, for use by the address select circuit 320. The DATA leads 207 and RETURN PARITY leads 223 are monitored by a check data parity circuit 510. In the event of a parity error in signals on either of the leads 207 and the leads 223, the check data parity circuit 510 generates a parity error signal on a parity error lead 511. A packet byte counter 512 is initiated at a zero count with each occurrence of the grant flag on the GRANT lead 214. The packet byte counter 512 counts clock signals on the CLOCK lead 217 and in the event that it reaches a count of 4096 it generates an overflow signal on an OVERFLOW lead 513. The overflow signal indicates that a Unit has reached an unexceptable maximum packet length in a single packet transmission. Each occurrence of the synchronous cycle signal on the SYNCHRONOUS CYCLE lead 215 inhibits the response of the counter 512 to the instant clock signal on the CLOCK lead 217. A multiplexer 516 gates the state of the ADDRESS leads 210 to a bus 517 except during an assertion of the synchronous cycle signal on the lead 215 whereupon the instant bus cycle count on the bus

401 is gated to the bus 517. A check control parity circuit 518 receives parity signals from the Terminator T on the CONTROL PARITY leads 222 and indicates a parity error on a parity error lead 519 in the event that at least one of the signals on the CONTROL PARITY leads 222 is asserted. Error registers 515 provide for temporary storage of error events as indicated on any of the leads 511, 513 and 519, and also provide for temporary storage of either the transmitting Unit's address or the bus cycle count at the instant of the error. If for example a parity error occurs on the DATA leads 207 during a synchronous cycle, the bus cycle count is stored and made available to the microprocessor 200. If for example an overflow error occurs, the address at the time of the last grant flag signal occurrence is made available to the microprocessor 200. In the event of either of a packet data parity error or an overflow, an abort circuit 514 asserts the abort signal.

Figure 6 illustrates one of the Repeaters R. Each of the Bus Controllers in figure 1 requires up to six Repeaters R for interfacing its Main Bus with up to six corresponding Segment Buses. Each Segment Bus includes leads labelled 221 - 225 each of which is wire connected to a single lead in a corresponding lead groups 221 - 225 in the Main Bus of the Bus Controller. The leads 209, 213, 214, 215, 218 in the Main Bus are coupled via amplifiers 640 - 644 to corresponding leads in the Segment Bus. The leads 216 and 217 are coupled via inverting amplifiers 645 and 646 to corresponding leads in the Segment Bus. In the Segment Bus the amplifier coupled leads are identified with corresponding units and ten digits in combination with the numeral six in the hundred digit position. Lower order ones of the ADDRESS leads 210 are amplifier coupled via amplifiers 650 to corresponding ADDRESS leads 610 in the Segment Bus. The remaining higher order ones of the ADDRESS leads 210 are decoded by a decoder 620 such that in the event that these higher order leads are of a signal state combination unique to the particular Repeater R a segment enable signal is asserted on an ENABLE lead 601. A data transfer control circuit includes AND gates 622 and 623, a JK flip-flop 624 and an OR gate 625 and an AND gate 628 connected as shown for controlling operation of receive signal transfer gates 626 and transmit signal transfer gates 627. The data transfer control circuit is responsive to a coincident occurrence of the grant flag signal and the segment enable signal in the case of packet transmission for permitting asynchronous signal transmission via the gates 627 to the DATA leads 207 of the main bus. In the case of synchronous signals a delayed synchronous request on one of the leads 420 is used by the AND gate 628 to gate the synchronous cycle signal to the OR gate 625 to cause signal transmission via the gates 627. Otherwise the gates 626 permit receive signal transmission to the DATA leads 607 of the Segment Bus.

The Segment Bus/Unit interface circuit in figure 7 is used to provide communication between a Unit and one of the Segment Buses. Two of these interface circuits are required for each Unit, one in connection with the Segment Bus A and the other in connection with the Segment Bus B. Each interface circuit provides for the data information transfer function and address and timing interface requirements for all types of Units be they of a synchronous or of an asynchronous nature.

In the Segment Bus/Unit interface circuit in figure 7 grant flag, clock, frame and synchronous cycle signals on leads 614 - 617 are gated, via inverting transmission gates 744 - 747, to corresponding leads 714 - 717 for use by an associated Unit under the control of the use signal on the USE lead 618 which is coupled to control ports thereof by an inverting amplifier 748. A HAND gate 724 generates a synchronous request signal on the SYNCHRONOUS REQUEST lead 224 in the Segment Bus in response to coincident occurrences of an advanced cycle match signal on a lead 760 and a synchronous required signal on a lead 761, from the associated Unit. A comparator 750 is connected to receive a slot number, which is defined by binary bit states in accordance with the physical location of the Segment Bus/Unit interface circuit in the network, and to receive the lower order bits of the address on the ADDRESS leads 610. The comparator 750 generates an address match signal at its output in response to the slot number and the address being equal in the presence of the segment enable signal on the lead 601. The output of the comparator 750 is connected as shown to a JK flip-flop 751, an AND gate 752, a NAND gate 753, an OR gate 755 and the inverting transmission gate 741. The address match signal is gated via the inverting transmission gate 741 to the lead 766 for use in the associated Unit. The JK flip-flop 751 provides a timing signal for gating a request signal from the associated Unit via a lead 763, and a NAND gate 721 to the REQUEST lead 221 in the Segment Bus. This timing signal is provided in response to an occurrence of the match signal and occurs coincident with the next occurring pulse of the clock signal as gated to the lead 716. Outputs of the gates 752 and 753 are connected to J and inverting K inputs of a JK flip-flop 757. A Q output of the JK flip-flop provides a gating signal for gating a done signal from the associated Unit via a lead 762 and a NAND gate 725 to the DONE lead 225 of the Segment Bus. The gating signal is also provided from an inverting Q output of the JK flip-flop 757 to an input of an OR gate 758. This gating

signal is initiated in response to a coincident occurrence of a pulse of the grant flag on the GRANT lead 614 and the address match signal from the comparator 750 at the time of the next following pulse of the clock signal on the lead 716. The gating signal is terminated in response to the next occurrence of the grant flag signal at the time of the next following pulse of the clock signal. The outputs of the respective NAND gate 721, 724 and 725 in each segment/unit interface circuit are WIRE ORed with those of the other segment/unit interface circuits connected to the segment bus.

The OR gate 758 also includes an input connected to receive a cycle match signal from the associated Unit via lead 764. Either of the gating signals from the JK flip-flop 757 or the cycle match signal from the lead 764 is coupled via the OR gate 758 to an input of an AND gate 723 and to an inverting input of an AND gate 722. The AND gates 722 and 723 each also include inverting inputs connected to the USE lead 618. Receive transmission gates 726 are used to couple data information signals from the DATA leads 607, in the Segment Bus to DATA leads 707 for reception by the associated Unit. Transmit transmission gates 727 are used to couple data information signals from the associated Unit, via the DATA leads 707, to the DATA leads 607. The receive transmission gates 726 are controlled from an output of the AND gate 722 to be ON in the presence of the use signal on the lead 618 while the output of the OR gate 758 is not asserted, and otherwise to be OFF. The transmit transmission gates 727 are controlled from an output of the AND gate 723 to be ON in the presence of the use signal while the output of the OR gate 758 is asserted and to otherwise be OFF. The RESET UNIT lead 613 of the Segment Bus is connected to an input of the OR gate 755, the output of which is connected to a D input of a D type flip-flop 756. The occurrence of a pulse of the reset signal coincident with the address match signal causes the flip-flop 756 to assert a reset signal at its inverting Q output at the moment of the next occurring clock pulse on the CLOCK lead 716. The reset signal is coupled to a reset lead 765 via the inverting gate 742 for use in the associated Unit.

Each of the Units shown in figure 1 have the ability to transmit and receive asynchronous data information signals via its associated Segment Bus/Unit interface circuit (figure 7) and the Segment Bus. Some of these Units may also have the capability of being able to transmit and receive synchronous data information signals. Such capability is required in cas s in which the Unit provides a port for a synchronous data stream in for example the T1 TDM format, or provides a port for one or more analog or digital telephone station sets. At least one of the remaining Units is the previously referred to call controller Unit. The call controller Unit includes a processor and program and data memories. Th call controller Unit is exemplary of various known central processing units, operable in accordance with stored program instructions, for controlling the setting up and tearing down of communication paths or channels in a telephone switching network. One suitable processor for this purpose is identified by device code 68000 and is available from Motorola. Of course an appropriate processor input/ output interface is required to interface any signal level and timing differences between the processor and the Segment Bus/Unit interface circuit. The synchronous Units require connection memory, for storing call set up information, supervisory status registers and the like, typical of a communication network port in a TDM telecommunication switching exchange. The structures and operations of the various types of the Units are not described as such will be apparent to persons of typical skill in the electronic arts pertaining to the structures and operations of digitally controlled TDM switching networks in view of the present disclosure and such communication features as said persons envisage.

In operation of the telecommunication switching network, inter and intra Unit communications are by way of the DATA leads in the Segment and Main Buses. Packetized data communications pertaining to information signals entering and leaving the network are communicated via the DATA leads between Units having an asynchronous communication capability. Synchonous data communications take priority over the packetized data communications and exclusively pertain to information signals entering and leaving the network. The synchronous data communications are always conducted between Units having a synchronous capability by way of the DATA leads. Destination identifications for all information signals entering and leaving the network are assigned by the call controller Unit in response to service rquests from the individual Units. Communication between each of the Units and the call controller Unit is by means of asynchronous packetized data which is also transmitted via the DATA leads. The call controller Unit has no other facility other than the DATA leads of the A and B Segment Buses for communicating with the other Units and the Main Buses.

A packetized data format is illustrated in figure 8. A data packet consists of up to 4096 words. Each word consists of eight binary bits plus a parity bit, not shown. The bits of each word are transmitted in parallel on the DATA leads. The words of the data packet are sequentially broadcast one word after the other throughout the telecommunications switching network. The first word of the packet includes a Security bit (7) which when

asserted indicates that the packet is a network control packet. A Null bit (6) is asserted solely by the Bus Controller to indicate a null packet and it prevents any of the Units from responding to the remainder of the word. Destination Module bits (4 - 0) specify which one of networks similar to the network of figure 1 the data packet is destined to be received in, and a Route bit (5) indicates which of up to two possible Inter Module Switch Units is designated for transmission of the data packet in the case where another network is specified by the Destination Module bit. The second word consists of Destination Unit Number (bits 7 - 0) which corresponds to a data address of the Unit for which the remainder of the words of the packet are intended for reception.

Any Unit receiving information for transmission in the form of packetized data via the telecommunications switching network first requests service by means of one or more data packets each having a header defining the call controller Unit as the destination of the data packet. Subsequently in response to the service request, the Call Controller Unit transmits a data packet having a header defining the requesting Unit as its destination. The packet also includes the destination address of the required receiving Unit. Subsequent to this the requesting Unit transmits the information in the form of one or more data packets, each data packet having a header as defined by the call controller Unit. The transmission of each packet is continuous with the possible exception of one or more temporary halts to permit one or more synchronous transmissions from one of more other Units.

The signal protocol by which access to the DATA leads is granted and packetized data is transmitted is illustrated in figure 9. Figure 9 includes eight time related rows which are illustrative of signals and functions as labelled together with bracketed numeric identifications of associated leads in the preceding figures. The nature of signals transmitted during each bus cycle on the DATA leads is exemplified by a row labelled DATA wherein null data is signified by the letter "N", synchronous data is signified by the letter "S", and each word of each data packet is indicated by a transmitting unit number followed by the word number in the data packet. Addresses are generated for the ADDRESS leads 210 by the poll and grant circuit 300. In this example address 0 - 191 are generated. Synchronous cycle occurrences are defined by the synchronous cycle signal on the SYNCHRONOUS CYCLE lead 215. In this example a request flag is asserted by the Unit, having a hardwired slot number 1, in the bus cycle following the address 1 occurrence. However as the DATA leads are not immediately available for data packet transmission due to synchronous transmission occurrences the DATA leads are not immediately granted to the Unit 1. Addressing continues until the DATA leads are available whereupon the address for the Unit 1, to which the DATA leads are granted, occurs simultaneously with the grant flag. It should be noticed that in this example a Unit of address 5 also requests access for a data packet transmission. In the bus cycle following the grant flag occurrence, the Unit 1 begins a packet transmission of which words one and two are header information consistent with figure 8. The Unit 1 transmits words one through five before being interrupted by a synchronous transmission occurrence. Three bus cycles later the Unit 1 transmits the sixth word and as it has only one word of its packet left to transmit, it generates a done flag on the DONE lead 225. Following yet another interruption by a synchronous transmission the last word of the packet is transmitted from the Unit 1 while at the same time the address for the Unit 5 and the grant flag are provided from the poll and grant circuit 300. The poll and grant circuit 300 immediately resumes polling for requests at address 16 and so on. After yet another synchronous transmission interruption the Unit 5 begins to transmit a data packet. As the microprocessor 200 has at some time recently detected some operational discontinuity in Unit 19, at the bus cycle in which the Unit 19 is addressed, the reset unit signal is asserted on the RESET UNIT lead 213 by the poll and grant circuit 300. All of the Units are capable of asynchronous communications in accordance with the protocol illustrated in figure 9, and although not shown include elastic storage queues, for transmission and reception of data packets, and appropriate call supervision and connection memory means.

In figure 10 the synchronous bus cycle protocol is illustrated. Figure 10 includes six time related rows which are illustrative of signals and functions as labelled together with bracketed numeric identification of associated leads in the preceding figures. The nature of signals transmitted during each bus cycle on the DATA leads is exemplified in a row labelled DATA wherein asynchronous data is signified by the letter "P" and synchronous data is signified by a numeric label corresponding to the instant bus cycle. The only relationship between the access protocol for packetized data and the synchronous bus cycle protocol is that with each occurrence of a synchronous transmission the packet access protocol is arrested as if time has ceased until synchronous transmission ceases whereupon the packet access protocol resumes exactly where it had left off. A frame signal pulse occurs with a period of one millisecond, during which time eight sub-frames of 640 bus cycles each occur. Synchronous cycle requests originate in individual ones of the units at times of

bus cycle occurrences having been defined by the Call controller Unit. Each synchronous cycle request occurs one bus cycle in advance of the moment when a synchronous cycle grant may be provided on the SYNCHRONOUS CYCLE lead 215, after which time, transmission of a single word occurs on the DATA leads. The transmitted word is received only by the Unit specified by the call controller Unit. Those of the Units capable of synchronous communication in accordance with the protocol illustrated in figure 10, also include circuit means for defining the bus cycle occurrences by number somewhat similar in function to the bus cycle counter 414 in figure 4, and appropriate supervision and connection memory means for synchronous signal calls.

The invention has been exemplified in the description of the example embodiment wherein a telecommunication time division multiplex switching network is alternately operable in either of asynchronous and synchronous information transfer modes. The invention is defined in the following claims.

Claims

1. A telecommunications switching network comprising:
a bus comprising a group of data leads for transmission of communications signals;
a plurality of units connected to the bus for transmitting and receiving asynchronous communication signals;
a bus controller comprising means for defining time slot intervals for transmitting and receiving between the bus and each of the units and for controlling access to the bus for transmitting the asynchronous communications signals;
characterized in that:
said bus controller further comprising means to define contiguously occurring frame intervals of a present number n of the time slot intervals each;
said plurality of units includes a call controller unit and at least one other unit capable of transmitting synchronous communication signals, the call controller being adapted to select one of the n time slot intervals and allocate said one time slot interval to said other unit in response to an asynchronous signal from said other unit representing a call set up request and said other unit being adapted to transmit synchronous signals in said allocated time slot interval, and to receive synchronous signals in a time slot allocated by the call controller unit;
whereby packetized data signals and synchronous signals may be interleaved during transmission via the bus.

2. A telecommunications switching network as defined in claim 1 wherein the bus controller comprises:
a poll means (310, 320) for polling the units for asynchronous transmission requests; and
grant means (350 - 380) for granting access to the data bus for an indefinite period of time, as required for transmission of a data packet from one of the units, sometime after an occurrence of an asynchronous transmission request from said one unit.

3. A telecommunications switching network as defined in claim 2 wherein the bus controller is connected to the units via a group of address leads (610) and a plurality of control leads (614 - 618, 221 - 225) and wherein:
the poll means includes an address counter (311) for periodically generating a series of addresses for polling the units one after the other via the address leads; and
the grant means includes a queue storage means (371) being responsive to an occurrence of an asynchronous transmission request in the form of a request flag having been asserted on a request of one of the control leads (221) by a polled unit for storing the address corresponding to the poled unit; and
wherein the bus controller further comprises:
an address select means (32)being responsive to at least one address having been stored in the queue storage means for inhibiting the address counter and for causing the address to be withdrawn from the queue storage means and asserted on the address leads coincident with generating a grant flag on a grant one of the control leads (214, 614).

4. A telecommunications switching network as defined in claim 3 wherein the poll means further comprises:
a poll range limiting means (312,313), being setable with first and second limits corresponding to limits of a range of addresses, for causing the address counter to be loaded with one of the limits in response to the counter having attained a count corresponding to the other of the limits, whereby in operation polling and subsequent grants may be limited to a population of less than a maximum possible number of units in the switching network.

5. A telecommunications switching network as defined in claim 3 or 4 wherein the grant means further comprises:
a disable unit address circuit (354) being setable with addresses for defining ones of the units being restricted from operation, and be-

ing responsive to an occurrence of a corresponding unit address on the address leads to prevent storage of the corresponding unit address in the queue storage means.

6. A telecommunications switching n twork as defined in claim 3, 4 and 5 wherein the grant means further comprises:
a wrap around circuit (357) being responsive to the request flag for preventing storage in the queue storage means of an address corresponding to an address presently stored in the queue storage means.

7. A telecommunications switching network as defined in claim 3, 4 or 5 wherein the grant means further comprises:
a wrap around circuit (357) includes a memory location corresponding to each of the addresses providable from the poll means, each memory location being operable to be set in the combined presence of its address and an assertion of the request flag and to be reset in the presence of its address while the request flag is unasserted and gating means (360) for generating an inhibit signal, in response to each address occurrence for which the corresponding memory location was set, for preventing storage of the corresponding address in the queue storage means.

8. A telecommunication switching network as defined in any of claims 2-7 wherein the bus controller further comprises:
a synchronous cycle means (400) being responsive to an occurrence of a synchronous request signal from any of the units, for generating a synchronous cycle signal for a predetermined time commencing at a pre-set time after said occurrence, for inhibiting any data packet transmission from any one of the units for and enabling a synchronous data transmission via the data leads during said predetermined period of time.

9. A telecommunication switching network as defined in claim 8 wherein the bus controller further comprises:
means (205) for generating clock and frame signals on clock and frame ones of control leads connecting the bus controller to the units, each frame signal having a period corresponding to a sum of a predetermined plurality of n clock signal periods; and
wher in the synchronous cycle means comprises:
a first gating circuit (412, 416) being setable to define a portion of each frame period within which synchronous cycle signals are permitted and in response to the clock and frame signals for generating an enable signal during each portion; and
a second gating circuit (410, 411, 412) being responsive to the clock signals and the enable signal for generating the synchronous cycle signal, on a synchronous cycle one of the control leads, being delayed a predetermined period of time from each occurrence of the synchronous request one of the control leads.

10. A telecommunications switching network as defined in claim 1 wherein the bus controller is connected to the units via a group of address leads (210) and a plurality of control leads (213 - 218, 221, 225) the bus controller comprising:
a timing circuit (205) for generating frame and clock signals, the clock signal having a period defining a period of a bus cycle, there being in clock signal periods in the period of the frame signal;
a selection circuit (320, 380) for selecting one of a poll circuit (310 - 316) and a grant circuit (370, 371, 378) as a source of addresses for transmission via the address leads in response to the clock signal, a state of a status signal from the grant circuit, and a done flag on a done one of the control leads;
a synchronous cycle circuit for defining bus cycle occurrences of zero through n during each frame period in response to the clock signal and frame signal, the synchronous cycle circuit being responsive to a synchronous request signal on a synchronous request one of the control leads (224) for asserting a synchronous cycle signal on a synchronous cycle one of the control leads (215) during a bus cycle in a setable range of the defined bus cycle occurrence;
the poll circuit comprising:
an address generating means (310, 313) for asserting addresses, within a setable range of addresses, one after another on the address bus and at the rate of the clock signal while selected by the selection circuit;
a grant circuit comprising:
a temporary storage means (350) for synchronizing an occurrence of a request flag signal on a request flag one of the control leads (221) with an associated address having already been received from the address bus;
a queue storage means (370, 378) for storing addresses from the temporary storag means one after another each storing being in respons to the presence of an associated request flag signal and for asserting the stored addresses on the address bus one after an-

other each assertion being in response to a grant flag from the select circuit on the grant one of the control leads (214), the queue storage means including at least one status output lead (375) being connected to the select circuit for indicating the queue storage means as being in one of a full state or an empty state.

11. A telecommunications switching network as defined in any one of claims 3-10 wherein each of the plurality of units is connected by a respective bus/unit interface circuit to transmit and receive call control signals and communication signals via the data leads, to be responsive to signals on various of the control leads and to originate signals on various of the control leads, the bus/unit interface circuit comprising:
matching means (750) for generating an address match signal for use in the unit in response to a correspondence between an address on the address leads and a preset address of the bus/unit interface circuit;
a request gating means (721, 751) for asserting the request flag on the request one of the control leads in response to a request signal from the unit and a pulse of the clock signal immediately following the address match signal from the matching means;
a grant latch (752, 753, 757) for generating a unit grant signal commencing with a pulse of the clock signal immediately following a coincidence of the grant flag on the grant one of the control leads and the address match signal from the matching means, and thereafter for terminating generation of the unit grant signal commencing with a pulse of the clock signal immediately following a subsequent occurrence of the grant flag;
a done gating means (725) for asserting the done flag signal on a done flag one of the control leads in response to a done unit signal from the unit occurring in the presence of the unit grant signal from the grant latch;
transmission gating means (722, 723, 726, 727, 758) for transmitting call control signals and/or communication signals from the unit to the data leads in response to either of the unit grant signal from the grant latch or a cycle match signal from the unit, and for alternately transmitting signals from the data leads to the unit in the absence of both the unit grant signal and the cycle match signal.

12. A telecommunications network as defined in any preceding claim wherein the data leads and the bus controller comprise a pair combination (A) which is duplicated (B) and wherein each of the units is connected via a pair of a bus/unit interface circuits to the data leads of each pair combination, each of the bus controllers including a use circuit (204) for arbitrating which of the bus controllers is active and inactive respectively, each use circuit being for generating a use signal i the absence of a use signal from the other bus controller for use by each of the bus/unit interface circuits for enabling communications between each unit and the data leads in current use.

13. A method of operating a telecommunication switching network, comprising the steps of:
providing an exclusive transmission privilege for a unit having a packetized message for transmission;
transmitting the packetized message while retaining said exclusive transmission privilege until the whole message has been transmitted;
the method being characterized by the steps of:
periodically providing a time slot for transmission from a unit with a synchronous transmission requirement;
and interrupting the transmission of a packetized message during each occurrence of said time slot, and resuming the transmission of the packetized message with the next occurrence of a time slot which has not been provided for a synchronous transmission requirement.

14. A method of operating a telecommunications switching network to provide for transmission of signals between units connected to a bus in the switching network wherein the signals include both asynchronous call control signals for transmission between a call controller one of the units and another of the units and communication signals for transmission between calling and called ones of the other units, the method comprising the steps of:
(a) in a bus controller arbitrating access to the bus for signal transmissions from the units by,
(i) polling the units for asynchronous transmission request and
(ii) granting access to the bus for an indefinite period of time to each unit having responded to being polled in step (i);
(b) generating frame and clock signals for defining frame periods each consisting of a plurality of bus cycles;
(c) in a unit requiring access to the bus for synchronous transmission, asserting a synchronous request signal at a predetermined time preceding a bus cycle having been

designated by the call controller unit and thereafter a communication signal on the bus during the designated bus cycle; and
in a unit defined by the call controller unit as a receiver during the designated bus cycle, receiving the communication signal from the bus during the designated bus cycle;
(d) in the remaining units including any unit having been granted access in step (ii), ceasing transmitting and/or reception throughout the duration of the designated bus cycle.

Revendications

1. Réseau de commutation de télécommunications comprenant :
   - un bus comprenant un groupe de fils de données pour transmission de signaux de communication;
   - une multitude d'unités connectées au bus pour transmettre et recevoir des signaux de communications asynchrones;
   - un contrôleur de bus comprenant un moyen pour définir des intervalles de secteurs temporels pour transmission et réception entre le bus et chacune des unités et pour commander l'accès au bus afin de transmettre les signaux de communications asynchrones;
   caractérisé en ce que :
   - le contrôleur du bus comprend en outre un moyen pour définir des intervalles de trames se produisant de manière contiguë d'un nombre présent n des intervalles de secteurs temporels chacun;
   - la multitude d'unités comprend une unité de commande d'appel et au moins une autre unité capable de transmettre des signaux de communication synchrones, le contrôleur d'appel étant destiné à sélectionner l'un des n intervalles de secteurs temporels et à affecter ledit intervalle de secteurs temporels à l'autre unité en réponse à un signal asynchrone provenant de l'autre unité qui représente une demande d'établissement d'appel et l'autre unité étant destinée à transmettre des signaux synchrones dans l'intervalle de secteur temporel affecté, et à recevoir des signaux synchrones dans un secteur affecté par l'unité d contrôleur d'appel;
   d'où il résulte que des signaux de données en paquets et des signaux synchrones peuvent être entremêlés pendant la transmission via le bus.

2. Système de commutation de télécommunications selon la revendication 1, dans lequel le contrôleur de bus comprend :
   - un moyen d'interrogation (310, 320) pour interroger les unités pour des demandes de transmission asynchrones; et
   - un moyen d'octroi (350 - 380) pour octroyer l'accès au bus de données pour un laps de temps indéfini, comme cela est nécessité pour la transmission d'un paquet de données à partir de l'une des unités, parfois après l'apparition d'une demande de transmission asynchrone à partir de ladite unité.

3. Système de commutation de télécommunications selon la revendication 2, dans lequel le contrôleur de bus est connecté aux unités via un groupe de fils d'adresses (610) et une multitude de fils de commande (614 - 618, 221 - 225) et dans lequel :
   - le moyen d'interrogation comprend un compteur d'adresses (311) pour produire périodiquement une série d'adresses pour interroger les unités l'une après l'autre via les fils d'adresses; et
   - le moyen d'octroi comprend un moyen de stockage de file d'attente (371) répondant à l'apparition d'une demande de transmission asynchrone sous la forme d'un indicateur de demande qui a été excité sur une demande de l'un des fils de commande (221) par une unité interrogée afin de stocker l'adresse correspondant à l'unité interrogée;
   et dans lequel le contrôleur de bus comprend en outre :
   - un moyen (32) de sélection d'adresses répondant à au moins une adresse qui a été stockée dans le moyen de stockage de file d'attente afin d'inhiber le compteur d'adresses et de provoquer l'extraction de l'adresse du moyen de stockage de file d'attente et excité sur les fils d'adresses en coïncidence avec la production d'un indicateur d'octroi sur un fil d'octroi des fils de commande (214, 614).

4. Réseau de commutation de télécommunications selon la revendication 3, dans lequel le moyen d'interrogation comprend en outre :
   - un moyen de limitation de la gamme d'interrogation (312, 313), pouvant être établi avec des première t seconde limites correspondant aux limites d'une gamme d'adresses, afin que le compteur d'adresses soit chargé avec l'une des

limites en réponse au fait que le compteur a atteint un comptage correspondant à l'autre des limites, d'où il résulte que pendant le fonctionnement, l'interrogation et les octrois successifs peuvent être limités à une population inférieure à un nombre maximum possible d'unités dans le réseau de commutation.

5. Réseau de commutation de télécommunications selon la revendication 3 ou 4, dans lequel le moyen d'octroi comprend en outre :
   - un circuit (354) d'adresses d'unité invalidée pouvant être établi avec des adresses pour définir des unités empêchées de fonctionner, et répondant à l'apparition d'une adresse d'unité correspondante sur les fils d'adresses afin d'éviter le stockage de l'adresse de l'unité correspondante dans le moyen de stockage de file d'attente.

6. Réseau de commutation de télécommunications selon la revendication 3, 4 et 5, dans lequel le moyen d'octroi comprend en outre :
   - un circuit de bouclage (357) répondant à l'indicateur de demande afin d'éviter le stockage dans le moyen de stockage de file d'attente d'une adresse correspondant à une adresse actuellement stockée dans le moyen de stockage de file d'attente

7. Réseau de commutation de télécommunications selon la revendication 3, 4 ou 5, dans lequel le moyen d'octroi comprend en outre :
   - un circuit de bouclage (357) qui comprend un emplacement de mémoire correspondant à chacune des adresses pouvant être fournie à partir du moyen d'interrogation, chaque emplacement de mémoire pouvant être établi dans la présence combinée de son adresse et d'une excitation de l'indicateur de demande et pouvant être remis à zéro en présence de son adresse alors que l'indicateur de demande n'est pas excité et un moyen de déclenchement (360) pour produire un signal d'inhibition, en réponse à chaque apparition d'adresse pour laquelle l'emplacement de mémoire correspondant a été établi, afin d'éviter le stockage de l'adresse correspondante dans le moyen de stockage de file d'attente.

8. Réseau de commutation de télécommunications selon l'une quelconque des revendications 2-7, dans lequel le contrôleur de bus comprend en outre :
   - un moyen de cycle synchrone (400) répondant à l'apparition d'un signal de demande synchrone provenant de l'une quelconque des unités, afin de produire un signal de cycle synchrone pendant une durée prédéterminée commençant à un instant préétabli suivant ladite apparition, afin d'inhiber toute transmission de paquets de données à partir de l'une quelconque des unités et pour valider une transmission de données synchrones via les fils de données pendant ladite durée prédéterminée.

9. Réseau de commutation de télécommunications selon la revendication 8, dans lequel le contrôleur de bus comprend en outre :
   - un moyen (205) pour engendrer des signaux d'horloge et de trame sur des fils d'horloge et de trame des fils de commande reliant le contrôleur du bus aux unités, chaque signal de trame ayant une période correspondant à la somme d'une multitude prédéterminée de n périodes de signaux d'horloge; et

   dans lequel le moyen de cycle synchrone comprend :
   - un premier circuit de déclenchement (412, 416) pouvant être établi de manière à définir une portion de chaque période de trame à l'intérieur de laquelle les signaux du cycle synchrone sont autorisés et en réponse aux signaux d'horloge et de trame pour produire un signal de validation lors de chaque portion; et
   - un second circuit de déclenchement (410, 411, 412) répondant aux signaux d'horloge et au signal de validation pour produire le signal de cycle synchrone, sur un cycle synchrone des fils de commande, retardé d'une durée prédéterminée par rapport à chaque apparition de la demande synchrone des fils de commande.

10. Réseau de commutation de télécommunications selon la revendication 1, dans lequel le contrôleur de bus est connecté aux unités via un groupe de fils d'adresses (210) et une multitude de fils de commande (213 - 218), 221, 225), le contrôleur de bus comprenant :
    - un circuit temporel (205) pour produir des signaux de trame et d'horloge, le signal d'horloge ayant une période définissant une période d'un cycle du bus, celle-ci étant dans les périodes du signal d'horloge dans la période du signal de

trame;

- un circuit de sélection (320, 380) pour sélectionner un circuit d'interrogation (310 - 316) ou un circuit d'octroi (370, 371, 378) comme source d'adresses pour transmission via les fils d'adresses en réponse au signal d'horloge, un état d'un signal d'état provenant du circuit d'octroi, et un indicateur exécuté sur un fil exécuté des fils de commande;
- un circuit de cycle synchrone pour définir les apparitions du cycle du bus de zéro jusqu'à n lors de chaque période de trame en réponse au signal d'horloge et au signal de trame, le circuit de cycle synchrone répondant à un signal de demande synchrone sur une demande synchrone de l'un des fils de commande (224) pour exciter un signal de cycle synchrone sur un fil synchrone de l'un des fils de commande (215) pendant un cycle du bus dans une gamme pouvant être établie de l'apparition définie du cycle du bus;

le circuit d'interrogation comprenant :

- un moyen générateur d'adresses (310, 313) pour exciter des adresses, à l'intérieur d'une gamme d'adresses pouvant être établie, l'une après l'autre sur le bus d'adresses et à une fréquence du signal d'horloge tout en étant choisies par le circuit de sélection;

un circuit d'octroi comprenant :

- un moyen de stockage temporaire (350) pour synchroniser une apparition d'un signal indicateur de demande sur un indicateur de demande de l'un des fils de commande (221) avec une adresse associée ayant déjà été reçue en provenance du bus d'adresses;
- un moyen de stockage de file d'attente (370, 378) pour stocker des adresses provenant du moyen de stockage temporaire, l'une après l'autre, chacune faisant le stockage en réponse à la présence d'un signal associé d'indicateur de demande et pour exciter les adresses stockées sur le bus d'adresses l'une après l'autre, chaque excitation s'effectuant en réponse à un indicateur d'octroi provenant du circuit de sélection sur le fil d'octroi des fils de commande (214), le moyen de stockage de file d'attente comprenant au moins un fil de sortie d'état (375) connecté au circuit de sélection pour indiquer que le moyen de stockage de file d'attente est à l'état complet ou à l'état vide.

11. Réseau de commutation de télécommunications selon l'une quelconque des revendications 3 à 10, dans lequel chaque unité de la multitude d'unités est connectée par un circuit respectif d'interface bus/unité afin de transmettre et de recevoir des signaux de commande d'appel et des signaux de communication via les fils de données, de manière à répondre à des signaux sur divers fils de commande et pour produire des signaux sur des fils divers de commande, le circuit d'interface bus/unité comprenant :
    - un moyen d'adaptation (750) pour générer un signal d'adaptation d'adresse pour emploi dans l'unité en réponse à une correspondance entre une adresse sur les fils d'adresse et une adresse préétablie sur le circuit d'interface bus/unité;
    - un moyen de déclenchement de demande (721, 751) pour exciter l'indicateur de demande sur le fil de demande parmi les fils de commande en réponse à un signal de demande provenant de l'unité et une impulsion du signal d'horloge suivant immédiatement le signal d'adaptation d'adresse provenant du moyen d'adaptation;
    - une bascule d'octroi (752, 753, 757) pour produire un signal d'octroi d'unité commençant avec une impulsion du signal d'horloge suivant immédiatement une coïncidence entre l'indicateur d'octroi sur le fil d'octroi parmi les fils de commande et le signal d'adaptation d'adresse provenant du moyen d'adaptation, et ensuite pour terminer la production du signal d'octroi d'unité commençant avec une impulsion du signal d'horloge suivant immédiatement une apparition ultérieure de l'indicateur d'octroi;
    - un moyen de déclenchement fait (725) pour exciter le signal d'indicateur fait sur un indicateur fait des fils de commande en réponse à un signal d'unité faite provenant de l'unité se produisant en présence du signal d'octroi d'unité provenant de la bascule d'octroi;
    - un moyen de déclenchement de transmission (722, 723, 726, 727, 758) pour transmettre des signaux de commande d'appel et/ou des signaux de communication entre l'unité et les fils de données en réponse soit au signal d'octroi d'unité provenant de la bascule d'octroi soit d'un signal d'adaptation de cycle provenant de l'unité, et pour transmettre alternativement des signaux entre les fils de données et l'unité en l'absence tant du si-

gnal d'octroi d'unité que du signal d'adaptation de cycle.

12. Réseau de télécommunications selon l'une quelconque des revendications précédentes, dans lequel les fils de données et le contrôleur du bus comprennent une combinaison par paire (A) qui est dupliquée (B) et dans lequel chacune des unités est connectée via une paire de circuits d'interface bus/unité aux fils de donnée de chaque combinaison par paire, chacun des contrôleur de bus comportant un circuit d'utilisation (204) pour arbitrer celui des contrôleurs du bus qui est actif et inactif respectivement, chaque circuit d'utilisation servant à produire un signal d'utilisation en l'absence d'un signal d'utilisation provenant de l'autre contrôleur du bus pour emploi par chacun des circuits d'interface bus/unité afin de permettre des communications entre chaque unité et les fils de données en utilisation courante.

13. Procédé pour faire fonctionner un réseau de commutation de télécommunications, comprenant les étapes consistant à :
- fournir un privilège de transmission exclusive pour une unité ayant un message sous forme de paquets pour transmission;
- transmettre le message en paquets tout en conservant le privilège de transmission exclusive jusqu'à ce que l'ensemble du message ait été transmis;
le procédé étant caractérisé par les étapes consistant à :
- fournir périodiquement un secteur temporel pour transmission à partir d'une unité avec une condition de transmission synchrone;
- et à interrompre la transmission d'un message en paquets pendant chaque apparition du secteur temporel, et à reprendre la transmission du message en paquets avec l'apparition suivante d'un secteur temporel qui n'a pas été fourni pour une condition de transmission synchrone.

14. Procédé pour faire fonctionner un réseau de commutation de télécommunications afin de fournir la transmission de signaux entre des unités connectées à un bus dans le réseau de commutation, dans lequel les signaux compr nn nt tant des signaux de command d'appel asynchrones pour transmission entre un contrôleur d'appel des unités et une autre des unités et des signaux de communication pour transmission ntr des unités appelant et appelée parmi les autres unités, le procédé comprenant les étapes consistant à :
(a) dans un contrôleur de bus, accéder arbitrairement au bus pour des transmissions de signaux à partir des unités en,
(i) interrogeant les unités pour une demande de transmission asynchrone; et
(ii) octroyant l'accès au bus pendant une durée indéfinie pour chaque unité ayant répondu à l'interrogation de l'étape (i);
(b) produire des signaux de trame et d'horloge afin de définir des périodes de trame, chacune étant constituée d'une multitude de cycles de bus;
(c) dans une unité demandant l'accès au bus pour une transmission synchrone, exciter un signal de demande synchrone à un instant prédéterminé précédant un cycle du bus ayant été désigné par l'unité du contrôleur d'appel et ensuite un signal de communication sur le bus pendant le cycle de bus désigné; et
dans une unité définie par l'unité du contrôleur d'appel comme récepteur pendant le cycle de bus désigné, recevoir le signal de communication provenant du bus pendant le cycle de bus désigné;
(d) dans les unités restantes, inclure toute unité qui s'est vue octroyer l'accès dans l'étape (ii), en cessant la transmission et/ou la réception pendant toute la durée du cycle du bus désigné.

Ansprüche

1. Nachrichtenfernverbindungs-Schaltnetz, das umfaßt:

einen Bus mit einer Gruppe von Datenleitungen zum Übertragen von Nachrichtensignalen;

eine Vielzahl von mit dem Bus verbundenen Einheiten zum Senden und Empfangen asynchroner Nachrichtenverbindungssignale;

eine Bussteuerung mit Mitteln zum Bestimmen von Zeitschlitzintervallen zum Senden und Empfangen zwischen dem Bus und jeder Einheit und zum Steuern des Zugriffs zum Bus zum Senden der asynchronen Nachrichtenverbindungssignale;

dadurch gekennzeichnet, daß:

die Bussteuerung weiter Mittel umfaßt, um aneinanderstoßend auftretende Rahmenintervalle einer vorhandenen Anzahl n von jeweiligen Zeitschlitzint rvallen zu b stimmen;

die Vielzahl von Einheiten eine Rufsteuerungseinheit von mindestens eine andere Einheit enthält, die zum Senden von synchronen Nachrichtenverbindungssignalen fähig ist, wobei die Rufsteuerung ausgelegt ist, einen der n Zeitschlitzintervalle auszuwählen und diesen einen Zeitschlitzintervallder anderen Einheit zuzuweisen in Abhängigkeit von einem asynchronen Signal von der anderen Einheit, das eine Rufeinricht-Anforderung darstellt, und die andere Einheit ausgelegt ist, synchrone Signale in dem zugeordneten Zeitschlitzintervall zu senden und synchrone Signale in einem Zeitschlitz zu empfangen, der durch die Rufsteuerungseinheit zugewiesen ist;

wodurch paketierte Datensignale und synchrone Signale während Sendung über den Bus miteinander verschachtelt werden können.

2. Nachrichtenfernverbindungs-Schaltnetz nach Anspruch 1, bei dem die Bussteuerung umfaßt:

ein Aufrufmittel (310, 320) zum Aufrufen der Einheiten zu asynchronen Sendeanforderungen; und

Gewährmittel (350-380) zum Gewähren von Zugriff zu dem Datenbus während einer unbestimmten Zeitlänge, wie sie zum Senden eines Datenpakets von einer der Einheit erforderlich ist, etwas nach einem Auftreten einer asynchronen Sendeanforderung von der einen Einheit.

3. Nachrichtenfernverbindungs-Schaltnetz nach Anspruch 2, bei dem die Bussteuerung mit den Einheiten über eine Gruppe von Adreßleitungen (610) und eine Vielzahl von Steuerleitungen (614-618,221-225) verbunden ist, und wobei:

das Aufrufmittel einen Adreßzähler (311) zum periodischen Erzeugen einer Reihe von Adressen enthält, um die Einheiten nacheinander über die Adreßleitungen aufzurufen; und

das Gewährmittel ein Warteschlangen-Speichermittel (371) enthält, das auf ein Auftreten einer asynchronen Sendeanforderung in Form eines Anforderungsmerkers reagiert, das auf eine Anforderung von einer der Steuerleitung (221) durch eine aufgerufen Einheit behauptet wurde zum Speichern der der aufgerufenen Einheit entsprechenden Adr sse; und die Bussteuerung weiter umfaßt:

ein Adressenauswahlmittel (32), das auf das Speichern mindestens einer Adresse in dem Warteschlangen-Speichermittel reagiert zum Sperren des Adreßzählers, und um die Adresse von dem Warteschlangen-Speichermittel zurückziehen zu lassen und sie an den Adreßleitungen zu behaupten, zusammenfallend mit der Erzeugung eines Gewährmerkers an einer gewährten Steuerleitung (214,614).

4. Nachrichtenfernverbindungs-Schaltnetz nach Anspruch 3, bei dem das Aufrufmittel weiter umfaßt:

ein Aufrufbereich-Begrenzungsmittel (312,313), das mit ersten und zweiten Grenzen entsprechend den Grenzen eines Adreßbereichs setzbar ist, um den Adreßzähler mit einer der Grenzen in Abhängigkeit davon beladen zu lassen, daß der Zähler einen der anderen Grenze entsprechenden Zählwert erreicht hat, wodurch im Betrieb Aufrufen und darauffolgendes Gewähren auf eine Population von weniger als einer maximal möglichen Anzahl von Einheiten im Schaltnetz begrenzt werden kann.

5. Nachrichtenfernverbindungs-Schaltnetz nach Anspruch 3 oder 4, bei dem das Gewährmittel weiter umfaßt:

einen Sperreinheitadreßkreis (354), der mit Adressen setzbar ist, um einzelne Einheiten als nicht zum Betrieb zugelassen zu bestimmen, und der auf das Aufteten einer entsprechenden Einheitenadresse an den Adreßleitungen reagiertmit Verhindern des Speicherns der entsprechenden Einheitenadresse in dem Warteschlangen-Speichermittel.

6. Nachrichtenfernverbindungs-Schaltnetz nach einem der Ansprüche 3, 4 oder 5, bei dem das Gewährmittel weiter umfaßt:

eine Umwickelschaltung (357), die auf den Anforderungsmerker reagiert, um das Einspeichern einer Adresse in das Warteschlangen-Speichermittel zu verhindern, die einer zur Zeit in dem Warteschlangen-Speichermittel gespeicherten Adresse entspricht.

7. Nachrichtenfernverbindungs-Schaltnetz nach einem der Ansprüche 3, 4 oder 5, bei dem das Gewährmittel weiter umfaßt:

eine Umwickelschaltung (357), welche einen Speicherplatz enthält entsprechend jeder Adresse, die von dem Aufrufmittel vorsehbar ist, wobei jeder Speicherplatz betätigbar ist, in die kombinierte Anwesenheit seiner Adresse

und einer Behauptung des Anforderungsmerkers gesetzt zu werden und rückgesetzt werden in die Anwesenheit seiner Adresse, während der Anforderungsmerker nicht behauptet ist, und Tormittel (360) zum Erzeugen eines Sperrsignals in Reaktion auf jedes Auftreten einer Adresse, für welche der entsprechende Speicherplatz gesetzt wurde, um Einspeichern der entsprechenden Adresse in das Warteschlangen-Speichermittel zu verhindern.

8. Nachrichtenfernverbindungs-Schaltnetz nach einem der Ansprüche 2 bis 7, bei dem die Bussteuerung weiter umfaßt:

ein Synchronzyklusmittel (400), das auf das Auftreten eines Synchronanforderungssignals von einer der Einheiten reagiert zum Erzeugen eines synchronen Zyklussignals während einer vorbestimmten Zeit, die an einem vorgesetzten Zeitpunkt nach dem Auftreten beginnt, um irgendeine Datenpaket-Sendung von einer Einheit zu sperren für eine Synchrondatensendung, und diese während des vorbestimmten Zeitraums über die Datenleitungen freizugeben.

9. Nachrichtenfernverbindungs-Schaltnetz nach Anspruch 8, bei dem die Bussteuerung weiter umfaßt:

Mittel (205) zum Erzeugen von Takt- und Rahmensignalen an Takt- und Rahmensteuerleitungen, welche die Bussteuerung mit den Einheiten verbinden, wobei jedes Rahmensignal eine einer Summe einer vorbestimmten Vielzahl von n Taktsignal-Zeitlängen entsprechende Zeitlänge besitzt; und

wobei das Synchronzyklusmittel umfaßt:

eine erste Torschaltung (412,416), die setzbar ist zum Bestimmen eines Abschnitts jeder Rahmenzeitlänge, innerhalb dessen synchrone Zyklussignale zugelassen sind, und um in Reaktion auf die Takt- und Rahmensignale ein Freigabe-Signal während jedes Abschnitts zu erzeugen; und

eine zweite Torschaltung (410,411,412), die auf die Taktsignale und das Freigabe-Signal reagiert mit Erzeugen des synchronen Zyklussignals an einem Synchronzyklus einer der Steuerleitungen, das eine vorbestimmten Zeitlänge gegen jedes Auftreten der Synchronanforderung einer der Steuerleitungen verzög rt ist.

10. Nachrichtenfernverbindungs-Schaltnetz nach Anspruch 1, bei dem die Bussteuerung mit den Einheiten über eine Gruppe von Adreßleitungen (210) und eine Vielzahl von Steuerleitungen (213-218,221,225) verbunden ist, wobei die Bussteuerung umfaßt:

eine Zeitgabeschaltung (205) zum Erzeugen von Rahmen- und Taktsignalen, wobei das Taktsignal eine Länge besitzt, die eine Zeitlänge eines Buszyklus bestimmt, und n Taktsignal-Zeitlängen in der Zeitlänge des Rahmensignals sind;

eine Auswahlschaltung (320,380) zum Auswählen einer Aufrufschaltung (310-316) und eine Gewährschaltung (370, 371,378) als eine Adreßquelle zum Senden über die Adreßleitungen in Reaktion auf das Taktsignal eines Zustands von einem Statussignal von der Gewährschaltung und eines "Erledigt"-Merkers an eine "Erledigt"-Steuerleitung;

eine Synchronzyklus-Schaltung zur Bestimmung von Buszyklus-Auftreten von Null bis einschließlich n während jeder Rahmenzeitlänge in Reaktion auf das Taktsignal und Rahmensignal, wobei die Synchronzyklus-Schaltung auf ein Synchronanforderungssignal an einer Synchronanforderungs-Steuerleitung (224) reagiert zum Behaupten eines Synchronzyklus-Signals an einer Synchronzyklus-Steuerleitung (215) während eines Buszyklus in einem setzbaren Bereich des bestimmten Buszyklus-Auftretens;

und die Aufrufschaltung umfaßt:

ein Adreßerzeugermittel (310,313) zum Behaupten von Adressen innerhalb eines setzbaren Bereichs von Adressen eine nach der anderen an dem Adreßbus und mit der Rate des Taktsignals, während sie durch die Auswahlschaltung ausgewählt sind;

eine Gewährschaltung, welche umfaßt:

ein Temporär-Speichermittel (350) zum Synchronisieren eines Auftretens eines Anforderungs-Merkersignals an einer Anforderungsmerker-Steuerleitung (221) mit einer zugehörigen Adresse, die schon vom Adreßbus empfangen wurde;

ein Warteschlangen-Speichermittel (370,378) zum aufeinanderfolgenden Speichern von Adressen von dem Temporär-Speichermittel, wobei jedes Speichern in Reaktion auf die An-

wesenheit eines zugeordneten Anforderungs-Merk rsignals geschieht und um die gespeicherten Adressen an dem Adreßbus eine nach der anderen zu behaupten, wobei jede Behauptung in Reaktion auf einen Gewährmerker von dem Auswahlkreis an der Gewähr-Steuerleitung (214) geschieht, und das Warteschlangen-Speichermittel mindestens eine Status-Ausgangssignal-Leitung (375) enthält, die mit der Auswahlschaltung verbunden ist zum Anzeigen, ob das Warteschlangen-Speichermittel entweder in einem vollen oder in einem leeren Zustand ist.

11. Nachrichtenfernverbindungs-Schaltnetz nach einem der Ansprüche 3 bis 10, bei dem jede aus der Vielzahl von Einheiten durch eine jeweilige Bus/Einheiten-Schnittstellenschaltung mit Sende- und Empfangs-Rufsteuersignalen und Verbindungssignalen über die Datenleitungen verbunden ist, um auf Signale an verschiedenen Steuerleitungen zu reagieren und Signale an verschiedenen Steuerleitungen entstehen zu lassen, wobei die Bus/Einheiten-Schnittstellenschaltung umfaßt:

Paßmittel (750) zur Erzeugung eines Adreßpaßsignals zur Verwendung in der Einheit in Reaktion auf eine Übereinstimmung zwischen einer Adresse an den Adreßleitungen und einer vorgegebenen Adresse der Bus/Einheiten-Schnittstellenschaltung;

ein Anforderungs-Tormittel (721,751) zum Behaupten des Anfordermerkers an der Anforder-Steuerleitung in Reaktion auf ein Anforderungssignal von der Einheit und einen Impuls des Taktsignals, der unmittelbar dem Adreßpaßsignal von dem Paßmittel folgt;

einen Gewähr-Riegelkreis (752,753,757) zum Erzeugen eines Einheiten-Gewährsignals, beginnend mit einem Impuls des Taktsignals, der unmittelbar einer Koinzidenz des Gewährmerkers an der Gewähr-Steuerleitung und des Adreßpaßsignals von dem Paßmittel folgt, und um danach die Erzeugung des Einheiten-Gewährsignals zu beenden, beginnend mit einem Impuls des Taktsignals unmittelbar folgend einem nachfolgenden Auftreten des Gewährmerkers;

ein "Erledigt"-Tormittel (725) zum Behaupten des "Erledigt"-Merkersignals an einer "Erledigt"-Merker-Steuerleitung in Abhängigkeit von einem "Erledigt"-Einheitensignal von der Einheit, das in Anw senheit d s Einheiten-Gewährsignals von dem G währriegelkreis auftritt;

Sendetormittel (722,723,726,727,758) zum Senden von Rufsteuersignalen und/oder Nachrichtungsverbindungs-Signalen von der Einheit zu den Datenleitungen in Abhängigkeit entweder von dem Einheiten-Gewährsignal von dem Gewährriegelkreis oder einem Zykluspaßsignal von der Einheit und zum abwechselnden Aussenden von Signalen von den Datenleitungen zu der Einheit in Abwesenheit sowohl des Einheiten-Gewährsignals als auch des Zyklus-Paßsignals.

12. Nachrichtenfernverbindungs-Schaltnetz nach einem der vorangehenden Ansprüche, bei dem die Datenleitungen und die Bussteuerung eine Paar-Kombination (A) umfassen, die dupliziert (B) ist, und wobei jede Einheit über ein Paar Bus/Einheiten-Schnittstellenschaltungen mit den Datenleitungen jeder Paar-Kombination verbunden ist, jede Bussteuerung eine Verwendungsschaltung (204) enthält zur Entscheidung, welche Bussteuerung jeweils aktiv bzw. inaktiv ist, jede Verwendungsschaltung zur Erzeugung eines Verwendungssignals in Abwesenheit eines Verwendungssignals von der anderen Bussteuerung vorhanden ist, zur Verwendung durch jede Bus/Einheiten-Schnittstellenschaltung zur Freigabe von Verbindungen zwischen jeder Einheit und den gegenwärtig verwendeten Datenleitungen.

13. Verfahren zum Betreiben eines Nachrichtenfernverbindungs-Schaltnetzes, mit den Schritten:

es wird ein exklusives Sendeprivileg für eine Einheit geschaffen, die eine paketierte Nachricht zu senden hat;

die paketierte Nachricht wird gesendet unter Aufrechterhaltung des exklusiven Sendeprivilegs, bis die gesamte Nachricht gesendet wurde;

wobei das Verfahren gekennzeichnet ist durch die Schritte:

es wird periodisch ein Zeitschlitz zu sendung von einer Einheit mit einer Synchronsendeanforderung geschaffen;

und das Senden einer paketierten Nachricht während jedes Auftretens des Zeitschlitzes unterbrochen und das Senden der paketierten Nachricht bei dem nächsten Auftreten eines Zeitschlitzes wieder aufg nomm n, der nicht

für eine Synchronsendeanforderung geschaffen worden ist.

14. Verfahren zum Betreiben eines Nachrichtenfernverbindungs-Schaltnetzes zum Einrichten des Sendens von Signalen zwischen Einheiten, die mit einem Bus im Schaltnetz verbunden sind, wobei die Signale sowohl asynchron Rufsteuersignale zur Sendung zwischen einer Rufsteuerung von einer Einheit zu einer anderen Einheit und Nachrichtenverbindungssignale zur Sendung zwischen rufenden und gerufenen anderen Einheiten enthalten, und das Verfahren die Schritte umfaßt:

(a) in einer Bussteuerung wird den Einheiten Zugriff zu dem Bus für Signalsendungen zugeteilt durch

(i) Aufrufen der Einheiten zur Asynchron-Sendeanforderung und

(ii) Gewähren von Zugriff zu dem Bus während einer unbestimmten Zeitlänge an jede Einheit, die bei dem Aufrufen in Schritt (i) geantwortet hat;

(b) Erzeugen von Rahmen- und Taktsignalen zum Bestimmen von Rahmenzeitlängen, die jeweils aus einer Vielzahl von Buszyklen bestehen;

(c) in einer Zugriff zu dem Bus zur Synchronsendung anfordernden Einheit, Behaupten eines Synchron-Anfordersignals zu einem vorbestimmten Zeitpunkt, der einem durch die Rufsteuereinheit bezeichneten Buszyklus vorangeht, und danach eines Nachrichtenverbindungssignals an dem Bus während des zugeordneten Buszyklus; und

in einer Einheit, die durch die Rufsteuereinheit als Empfänger während des zugeordneten Buszyklus bestimmt ist, Empfangen des Nachrichtenverbindungssignals von dem Bus während des zugeordneten Buszyklus;

d) in den restlichen Einheit einschließlich jeder Einheit, der im Schritt (ii) Zugriff gewährt wurde, Einstellen des Sendens und/oder des Empfangs während der gesamten Dauer des zugeordneten Buszyklus.

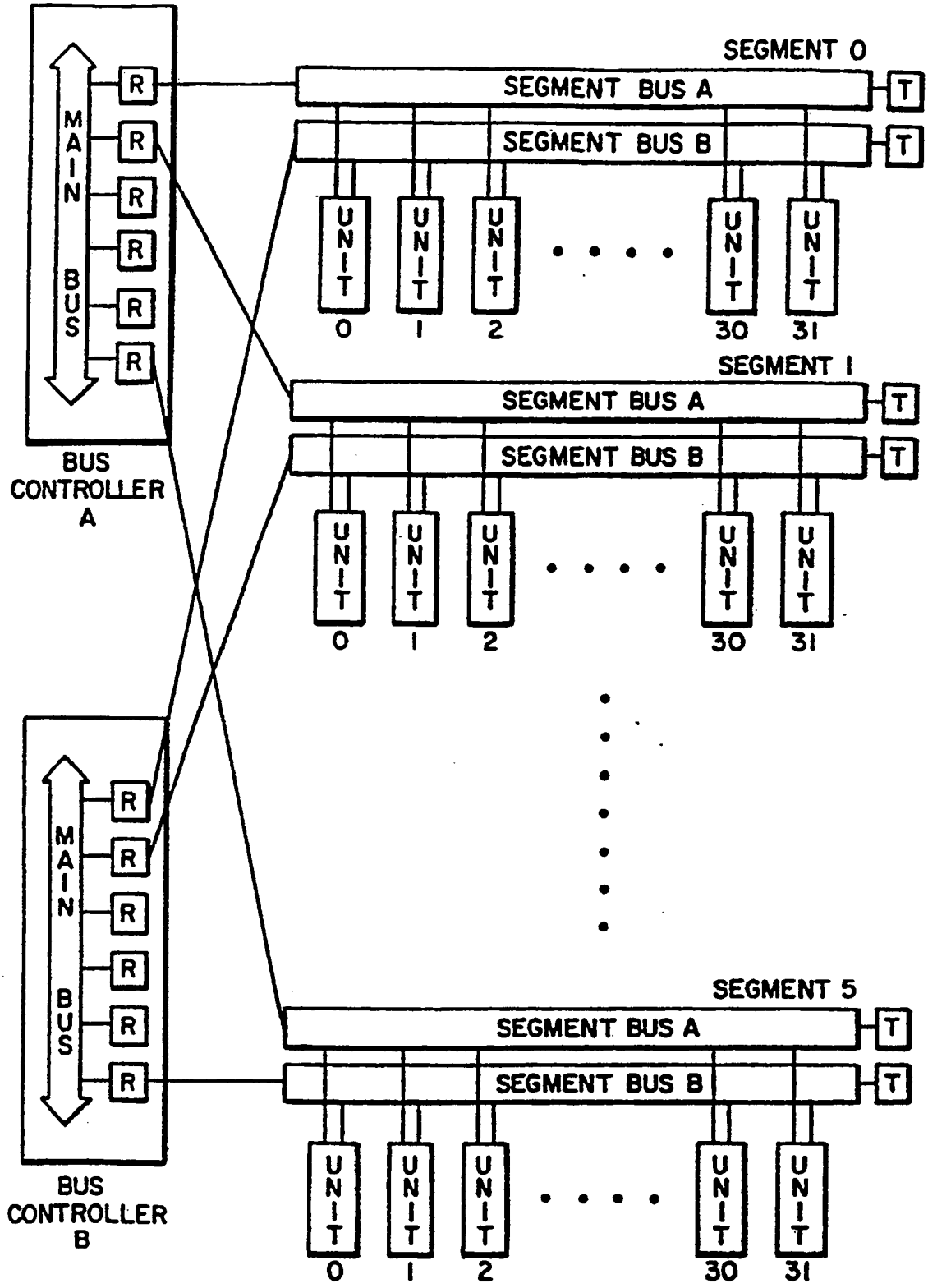
MAIN BUS
R
BUS CONTROLLER A
BUS CONTROLLER B
SEGMENT 0
SEGMENT BUS A
SEGMENT BUS B
T
UNIT 0
UNIT 1
UNIT 2
UNIT 30
UNIT 31
SEGMENT 1
SEGMENT 5

FIG. 1

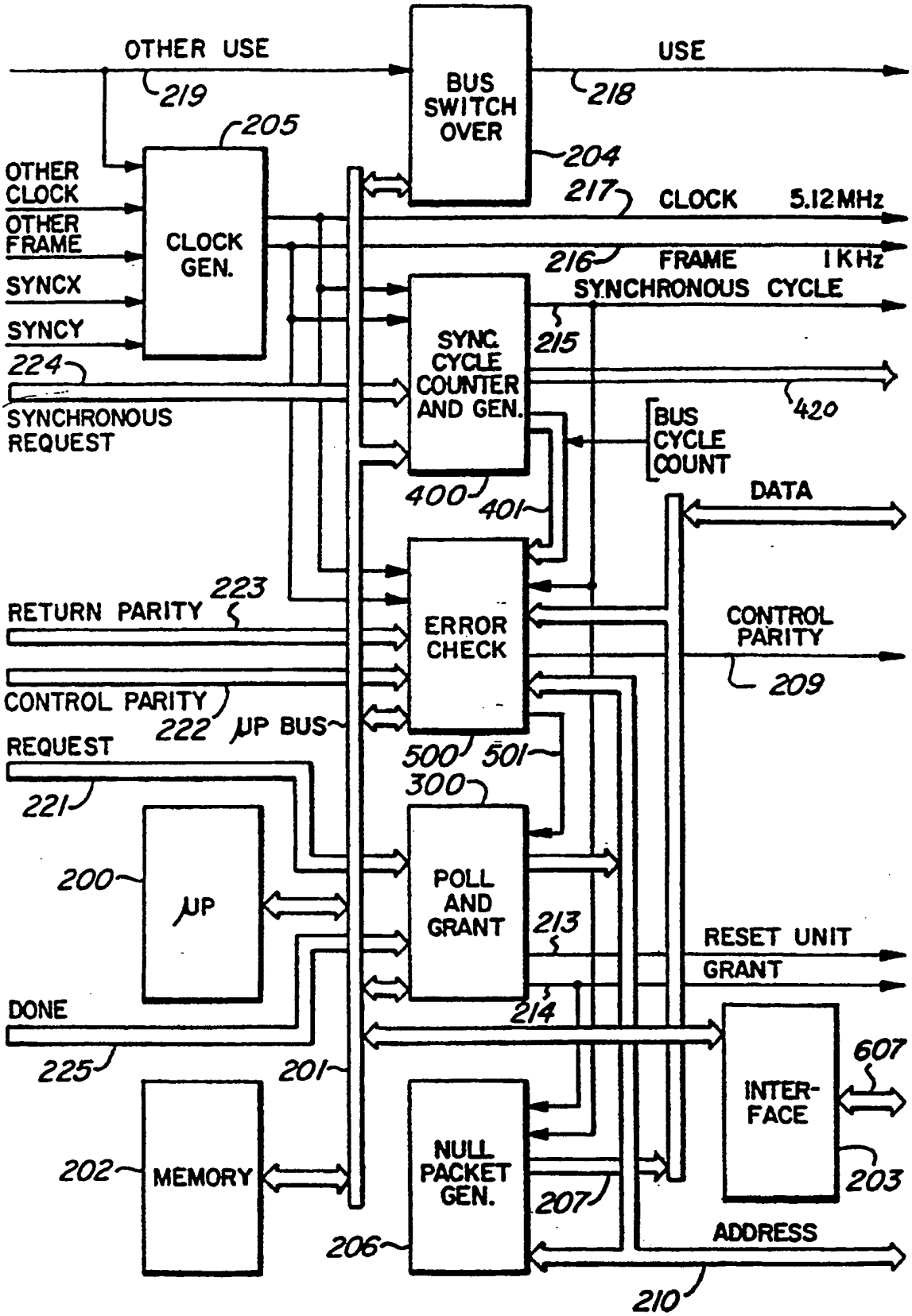
OTHER USE
219
BUS SWITCH OVER
USE
218
205
204
OTHER CLOCK
OTHER FRAME
SYNCX
SYNCY
CLOCK GEN.
217
CLOCK 5.12MHz
216
FRAME 1KHz
SYNCHRONOUS CYCLE
224
SYNCHRONOUS REQUEST
SYNC. CYCLE COUNTER AND GEN.
215
420
BUS CYCLE COUNT
400
401
DATA
223
RETURN PARITY
ERROR CHECK
CONTROL PARITY
209
CONTROL PARITY
222
μP BUS
REQUEST
500
501
300
221
200
μP
POLL AND GRANT
213
RESET UNIT
GRANT
DONE
214
225
201
607
INTER-FACE
202
MEMORY
NULL PACKET GEN.
207
203
206
ADDRESS
210

FIG. 2

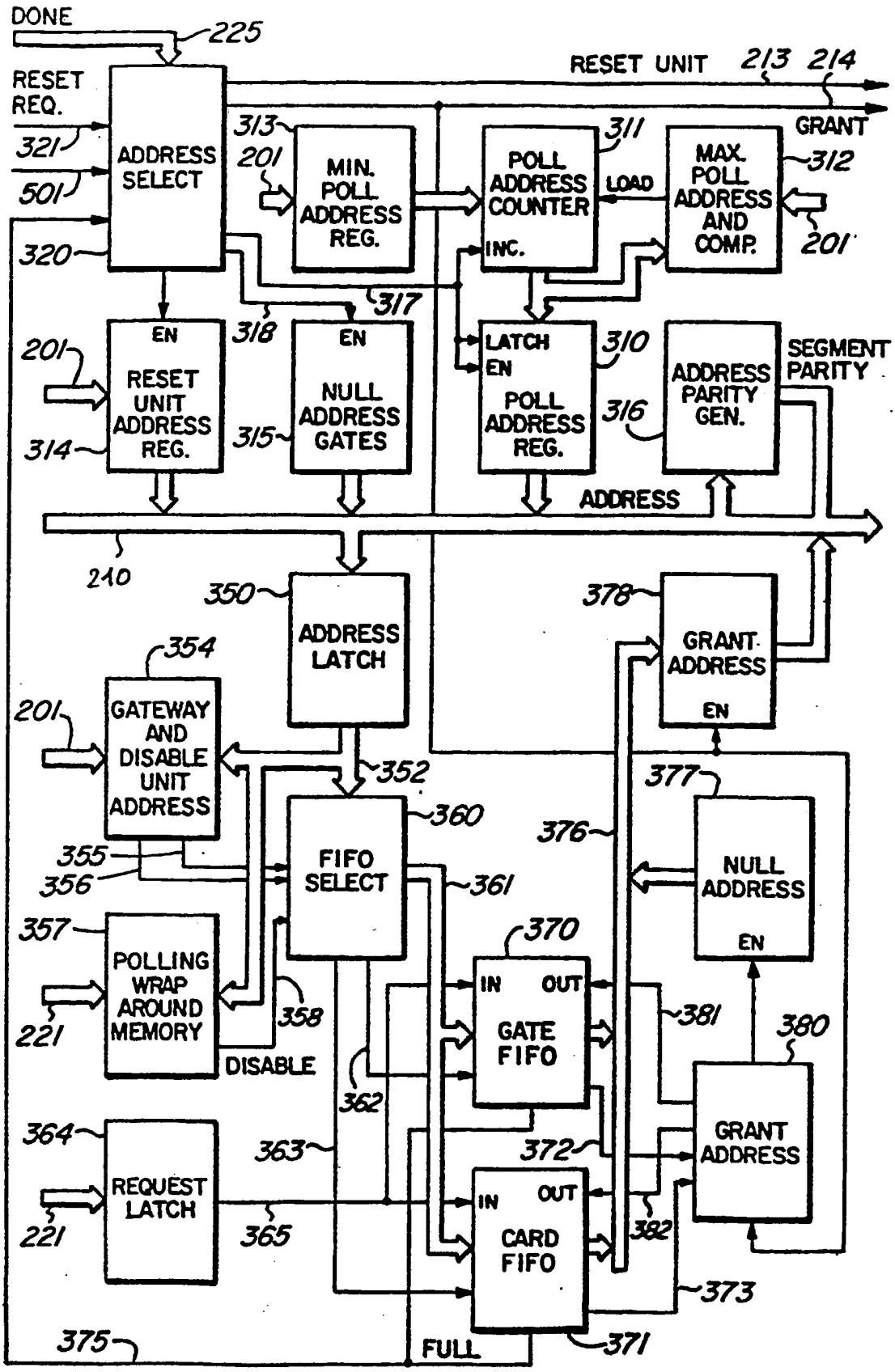
DONE
225
RESET UNIT
213
214
RESET REQ.
321
501
ADDRESS SELECT
320
313
201
MIN. POLL ADDRESS REG.
311
POLL ADDRESS COUNTER
LOAD
INC.
MAX. POLL ADDRESS AND COMP.
312
201
GRANT
317
318
EN
RESET UNIT ADDRESS REG.
201
314
EN
NULL ADDRESS GATES
315
LATCH EN
POLL ADDRESS REG.
310
316
ADDRESS PARITY GEN.
SEGMENT PARITY
ADDRESS
210
350
ADDRESS LATCH
378
GRANT ADDRESS
EN
354
201
GATEWAY AND DISABLE UNIT ADDRESS
352
377
360
376
355
356
FIFO SELECT
361
NULL ADDRESS
EN
357
370
POLLING WRAP AROUND MEMORY
221
358
DISABLE
IN
OUT
GATE FIFO
381
380
362
364
363
372
REQUEST LATCH
221
365
IN
OUT
CARD FIFO
382
GRANT ADDRESS
373
375
FULL
371

FIG. 3

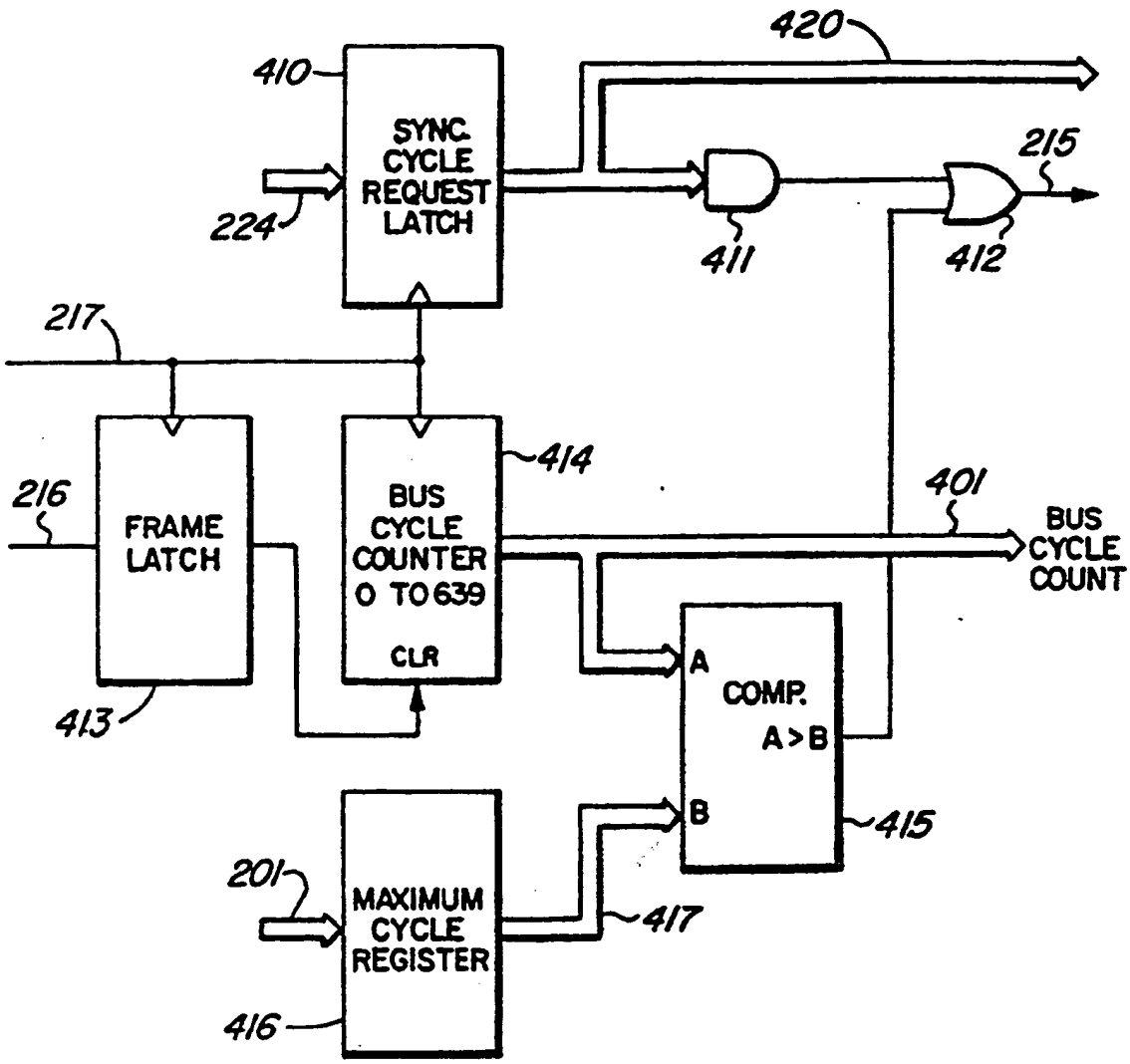
420
410
SYNC. CYCLE REQUEST LATCH
224
411
215
412
217
216
FRAME LATCH
413
BUS CYCLE COUNTER 0 TO 639
CLR
414
401
BUS CYCLE COUNT
A
COMP. A>B
B
415
201
MAXIMUM CYCLE REGISTER
416
417

FIG. 4

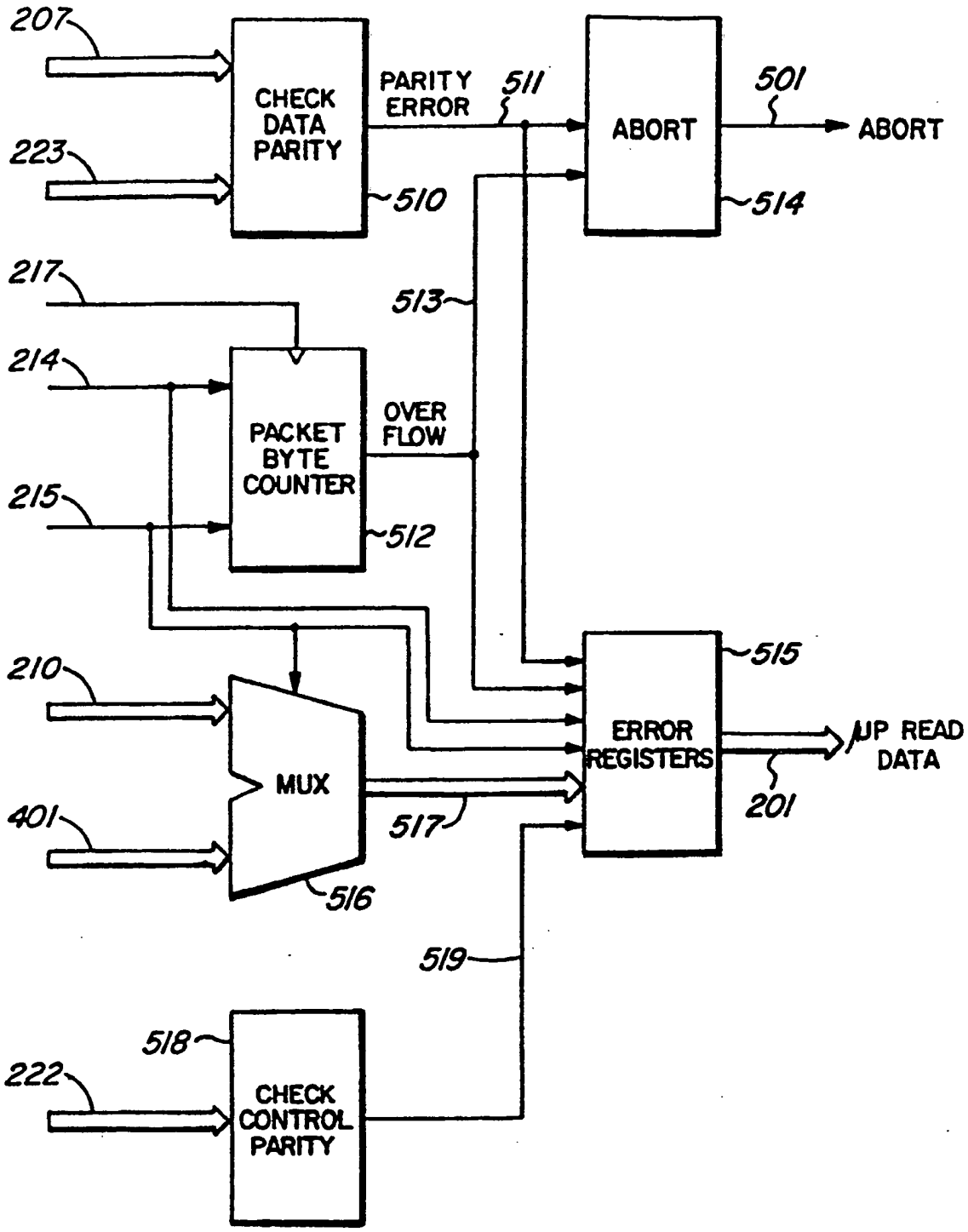
207
223
CHECK DATA PARITY
PARITY ERROR
511
510
ABORT
501
ABORT
514
217
513
214
PACKET BYTE COUNTER
OVER FLOW
215
512
210
MUX
401
516
517
ERROR REGISTERS
515
UP READ DATA
201
519
518
222
CHECK CONTROL PARITY

FIG. 5

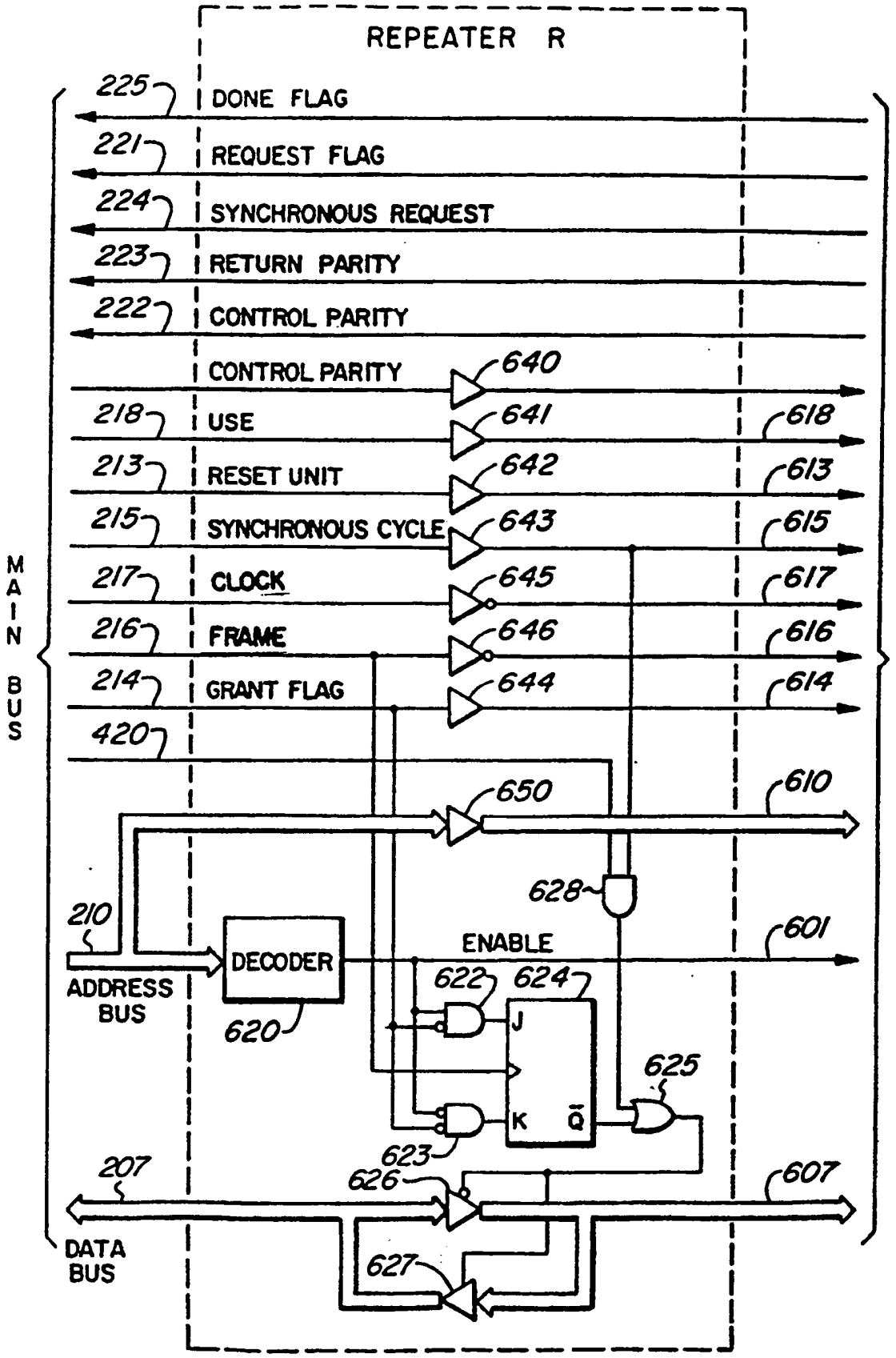
REPEATER R
225
DONE FLAG
221
REQUEST FLAG
224
SYNCHRONOUS REQUEST
223
RETURN PARITY
222
CONTROL PARITY
CONTROL PARITY
640
218
USE
641
618
213
RESET UNIT
642
613
215
SYNCHRONOUS CYCLE
643
615
217
CLOCK
645
617
216
FRAME
646
616
214
GRANT FLAG
644
614
420
650
610
628
210
ADDRESS BUS
DECODER
620
ENABLE
601
622
624
J
K
Q̄
625
623
626
207
607
DATA BUS
627
MAIN BUS
SEGMENT BUS

FIG. 6

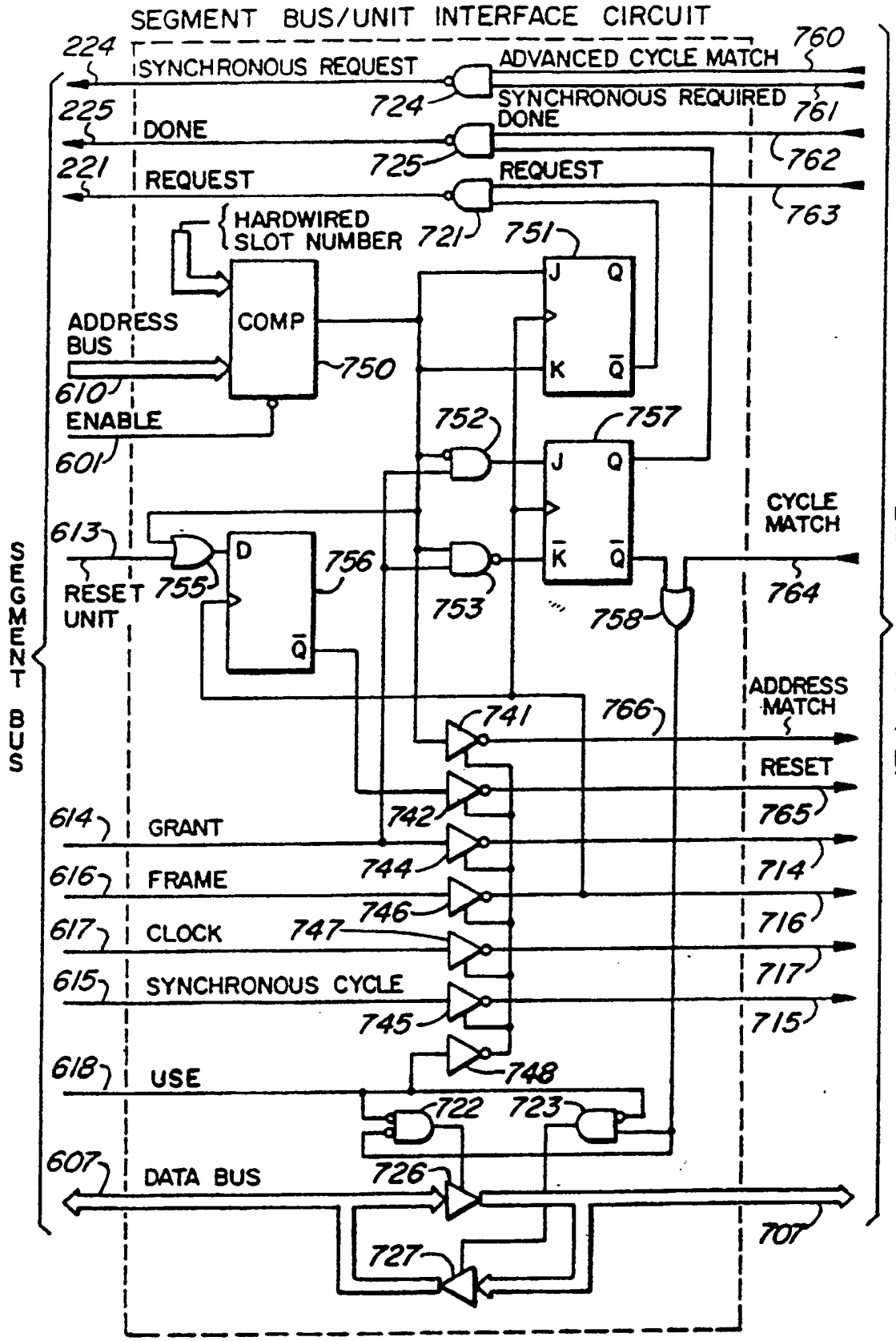
SEGMENT BUS/UNIT INTERFACE CIRCUIT
SEGMENT BUS
UNIT CIRCUITRY
224
SYNCHRONOUS REQUEST
724
ADVANCED CYCLE MATCH
760
SYNCHRONOUS REQUIRED
761
225
DONE
725
DONE
762
221
REQUEST
REQUEST
763
HARDWIRED SLOT NUMBER
721
751
J
Q
K
Q̄
ADDRESS BUS
COMP
750
610
ENABLE
601
752
757
613
D
756
RESET UNIT
755
753
758
CYCLE MATCH
764
Q̄
741
766
ADDRESS MATCH
RESET
765
614
GRANT
742
616
FRAME
744
714
617
CLOCK
746
747
716
615
SYNCHRONOUS CYCLE
745
717
715
618
USE
748
722
723
607
DATA BUS
726
707
727

FIG. 7

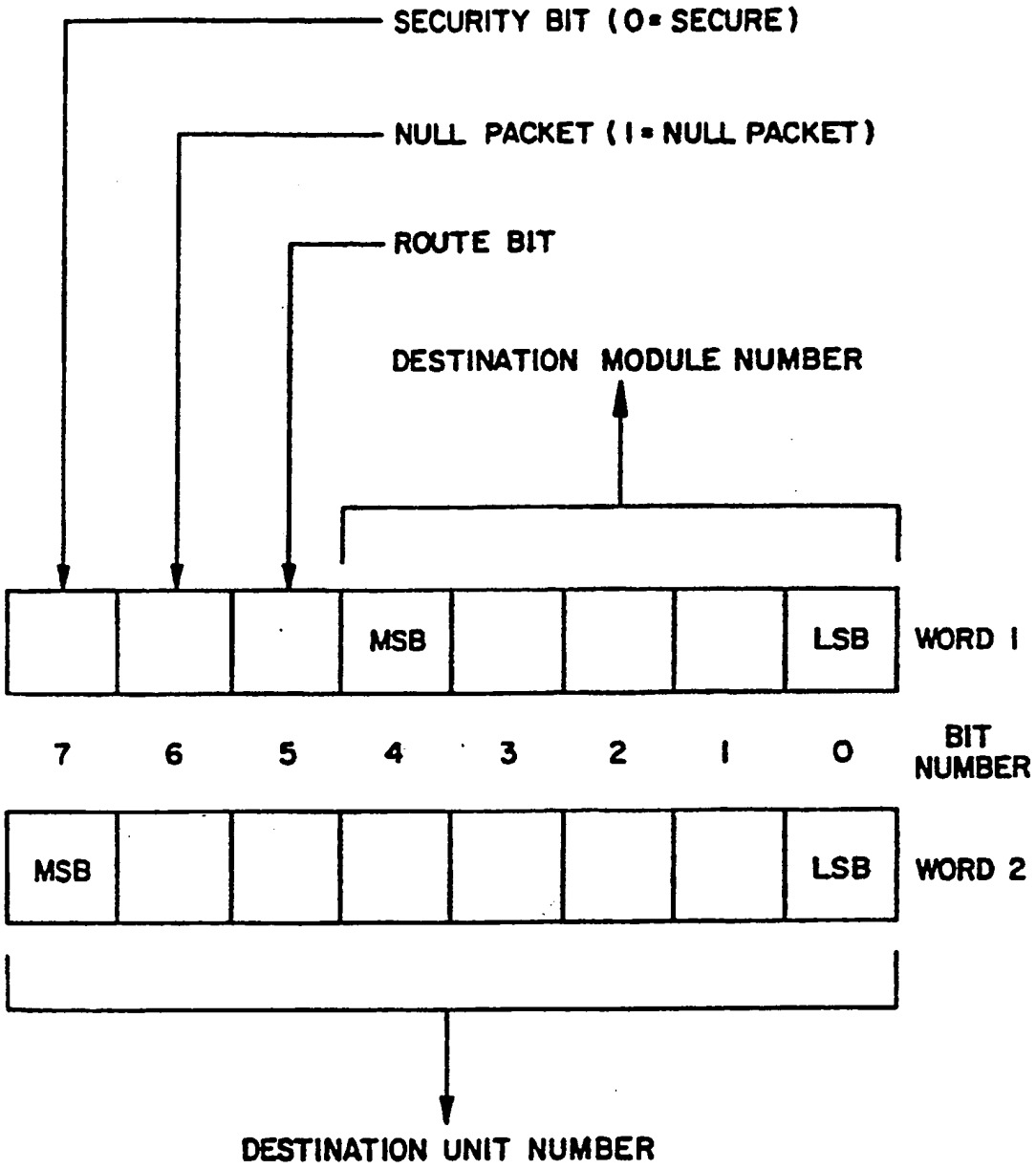
SECURITY BIT (0 = SECURE)
NULL PACKET (1 = NULL PACKET)
ROUTE BIT
DESTINATION MODULE NUMBER
MSB
LSB
WORD 1
7
6
5
4
3
2
1
0
BIT NUMBER
MSB
LSB
WORD 2
DESTINATION UNIT NUMBER

FIG. 8

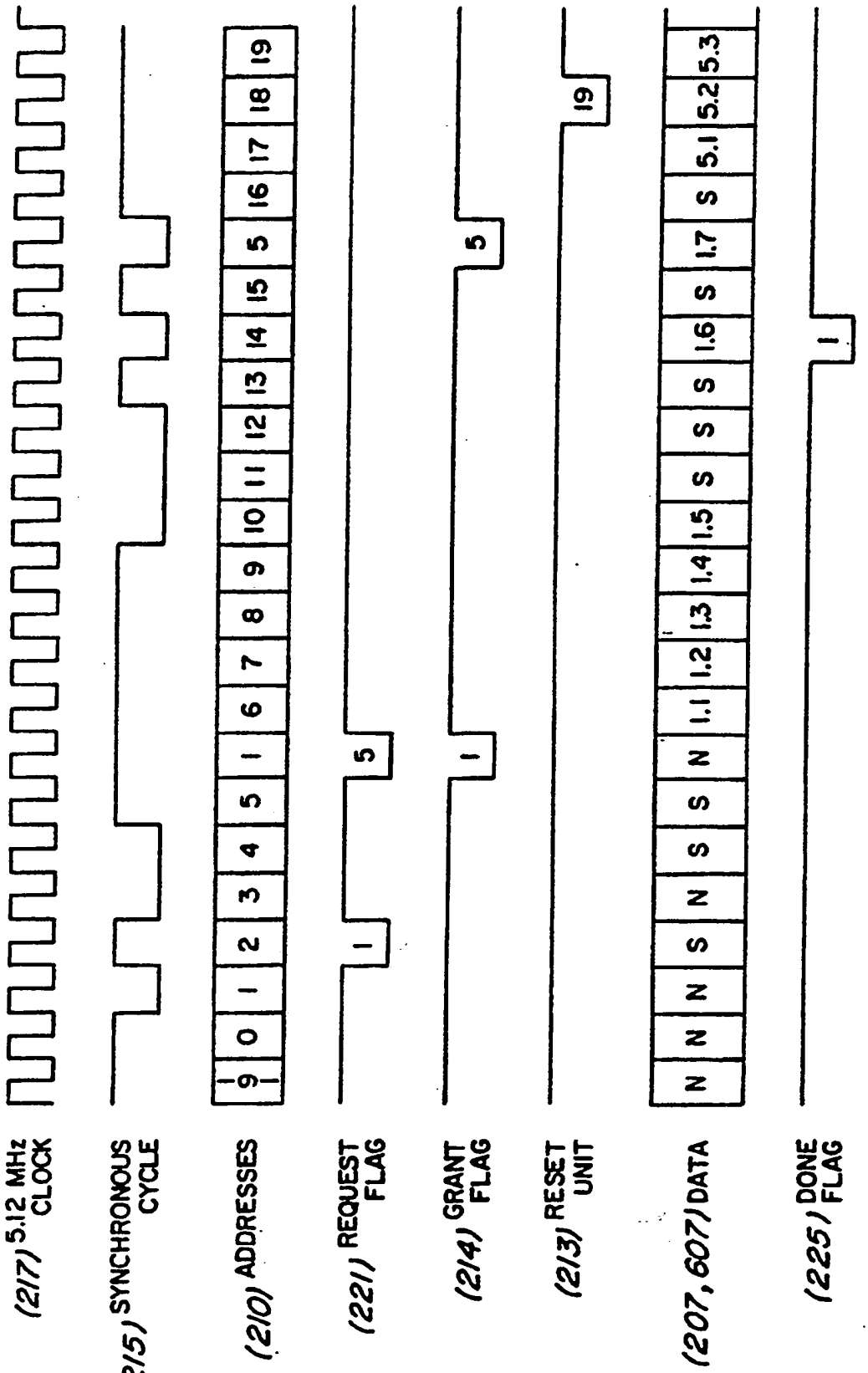
(217) 5.12 MHz CLOCK
(215) SYNCHRONOUS CYCLE
(210) ADDRESSES
(221) REQUEST FLAG
(214) GRANT FLAG
(213) RESET UNIT
(207, 607) DATA
(225) DONE FLAG

FIG. 9

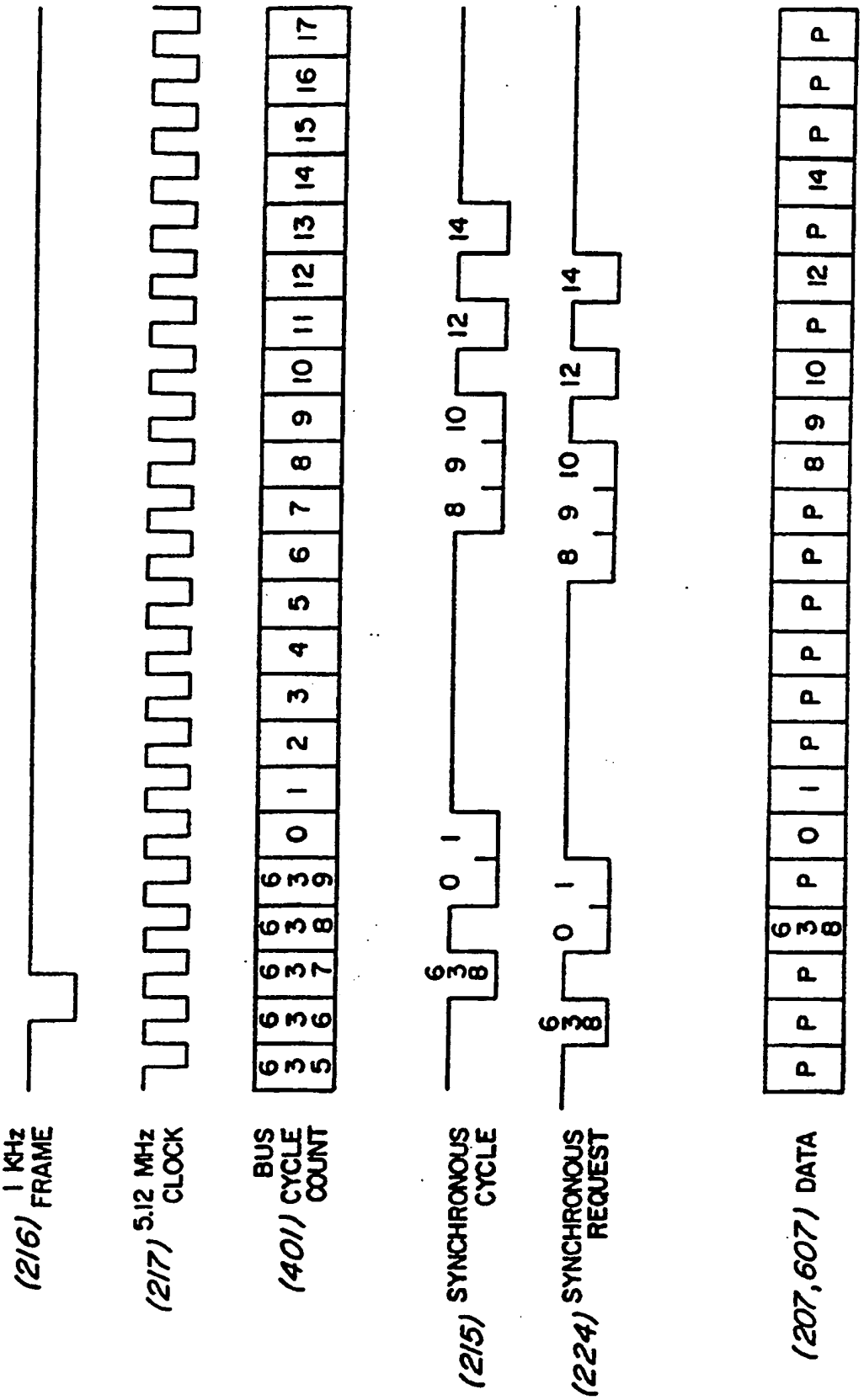
(216) 1 KHz FRAME
(217) 5.12 MHz CLOCK
(401) BUS CYCLE COUNT
(215) SYNCHRONOUS CYCLE
(224) SYNCHRONOUS REQUEST
(207, 607) DATA

FIG. 10